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Low-distortion 4th order programmable Butterworth filter

M. Teresa Sanz *, Santiago Celma, Belén Calvo

Grupo de Diseño Electrónico, Dpto. Ingeniería Electrónica y Comunicaciones, Facultad de Ciencias, Universidad de Zaragoza, Pedro Cerbuna 12, E-50009 Zaragoza, Spain

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Abstract

A highly linear 4th order low-pass filter with one decade frequency programmability and 39 dB gain programmability is presented in this paper. Low distortion is achieved through the use of the inherently linear current division principle. The paper provides the basic equations of the Butterworth filter and shows how to achieve programmability. A prototype was fabricated in a 0.35 μm–3.3 V CMOS process and experimental measurements prove the high linearity of the system. A distortion level better than −65 dB for 2 $V_{p\text{-}p}$ output signal is obtained.

1. Introduction

The presence of a massive digital core in mixed analogue-digital systems results in many complications on the analogue side, such as crosstalk noise contamination of the sensitive analogue signals or voltage supply downscale related issues, among others. Nevertheless, the designer can take advantage of the digital circuitry in the chip to implement high accuracy automatic gain control of the variable gain amplifier and digital tuning of the analogue filter. Digital programmability is thus becoming an essential feature for complex mixed-signal systems. The built-in DSP is often used to accurately compute the control signal for the reconfiguration of the analogue side. This technique eases operation at different gain settings and different bandwidths, which is demanded by many analog baseband circuits such as multistandard receivers [1] or hearing aid systems [2].

In all these applications, analogue pre-processing of the signal must offer at least the same accuracy as the associated A/D converters. In consequence, for some applications over the baseband and telecommunication ranges, a dynamic range of at least 60 dB and linearity better than −65 dB are necessary.

Unfortunately, it is not easy to achieve this performance with fully integrated circuits in current CMOS technologies and it becomes even more difficult as the operating frequency increases and supply voltage drops.

MOS resistive circuits [3–7] show distortion levels higher than −60 dB for 1 $V_{p\text{-}p}$ signal swing in single 5 V systems. Furthermore, the tuning capability of this approach is extremely limited for low-voltage systems, as the mechanism of tuning is based on the variation of the gate voltage of transistors operating in the triode region.

For low voltage compatibility, a possible solution is to use programmable arrays of polysilicon resistors and/or capacitors [8]. High linearity and dynamic range are achieved with this approach. Unfortunately, the maximum operating frequency is limited by the presence of MOS switches in the signal path. Furthermore, extensive area is needed to guarantee a minimum of accuracy [9].

An approach combining good linearity and moderate area consumption is the use of MOS transistor configurations which make use of the inherently linear current division principle [10].

This paper describes the principles, design and experimental results of a highly linear programmable 4th order Butterworth filter in standard CMOS technology for the

* Corresponding author. Tel.: +34 976761240; fax: +34 976762143.
E-mail addresses: materesa@unizar.es (M. Teresa Sanz), scelma@unizar.es (S. Celma), becalvo@unizar.es (B. Calvo).

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baseband frequency range. Section 2 describes a new highly linear programmable integrator. Starting from this cell, Section 3 describes a programmable biquadratic section and its application to realize a 4th order Butterworth filter. Experimental results are discussed in Section 4 and some conclusions are drawn in Section 5. Finally, a deeper explanation of the operation principle of the highly linear MOS Current Divider can be found in the appendix.

2. MOS Current Divider-based programmable integrator

Fig. 1 shows the proposed fully balanced programmable integrator. It is based on the MOST-only inherently linear current division principle reported in [10], where a linearity better than −85 dB was achieved for a volume control system in the audio frequency band. The key idea is that the accuracy of the current division does not depend on the linearity of the transistors (see appendix).

In this work, wide-band OTAs are employed and banks of MOS transistors in parallel constitute the current divider. Complementary words, $A(n) = \{a_n\ a_{n-1} \ldots\ a_0\}$ and $\overline{A}(n) = \{\bar{a}_n\ \ \bar{a}_{n-1}\ \ \ldots\ \ \bar{a}_0\}$, are applied to identical n-bit programmable transistor banks with binary weighted transistor sizes. The differential output voltage $V_o = V_o^+ - V_o^-$ can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{\Delta}{1-\Delta}\frac{1}{sCR}\eta \tag{1}$$

with

$$\Delta = \frac{1}{[m(2^n-1)+2]}\left(1 + m\sum_{j=0}^{n-1} a_j 2^j\right) \tag{2}$$

Factor m is the size ratio between transistors M_{a0} and M_a, i.e., $m = (W/L)_{a0}/(W/L)_a$. Factor η appears as a result of the influence of the finite OTA transconductance value G_m. If G_m is in the order of 100 mA/V for an equivalent load resistance $R_L = 10\ \text{k}\Omega$, then $\eta = 0.99$, that is, the OTA works as a wide-band operational amplifier with an error in gain of 1%.

A two-stage OTA with high transconductance and therefore resistor-driving capability was specifically designed as shown in Fig. 2. The source coupled differential pair which constitutes the second stage provides better substrate and common mode noise attenuation than a simple common source. Though not shown, a CMFB circuit and a temperature independent biasing circuit were used [11]. Tables 1 and 2 show transistor sizes and performance of the OTA, respectively.

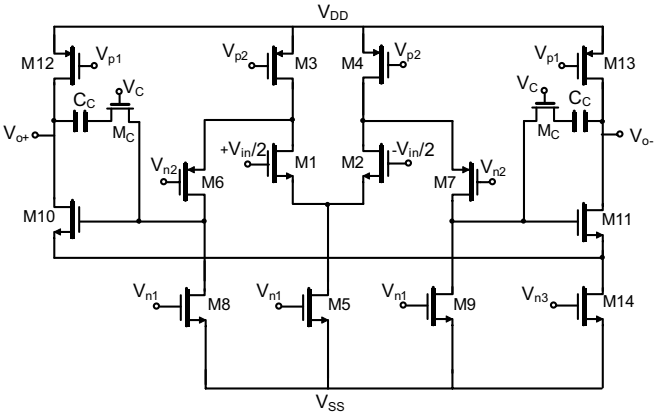

Fig. 2. Scheme of the fully-differential OTA (CMFB circuit omitted).

Table 1
OTA transistor sizes

Transistor	W/L (μm/μm)
M_1, M_2	67/0.4
M_3, M_4	62/0.4
M_5	18/0.4
M_6, M_7	18/0.4
M_8, M_9	14/0.7
M_{10}, M_{11}	314.5/0.4
M_{12}, M_{13}	163.1/0.4
M_{14}	42/0.4
M_C	36/0.35

Table 2
OTA performance summary

OTA parameter	Value
Supply voltage	2.5 V
G_m	2.3 A/V
Unity gain frequency ($R_L = 2\ \text{k}\Omega$)	148 MHz
Phase margin@$C_C = 3$ pF	65°
Differential output swing	3.0 V
Power consumption	7.3 mW
Settling time (10%–90%)	10 ns
THD (1 MHz@2$V_{p\text{-}p}$ output)	−88.6 dB
Input referred noise	104 μVrms
Dynamic range	82.7 dB

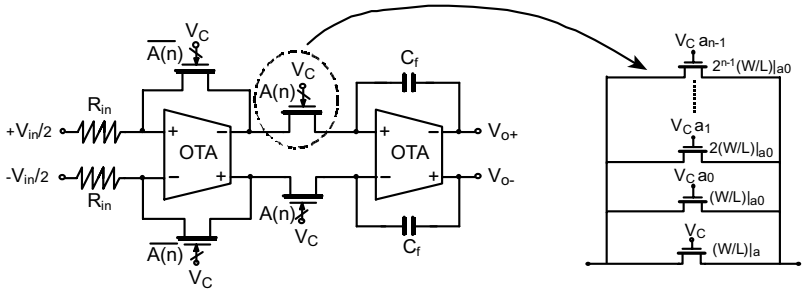

Fig. 1. MOS Current Divider-based integrator.

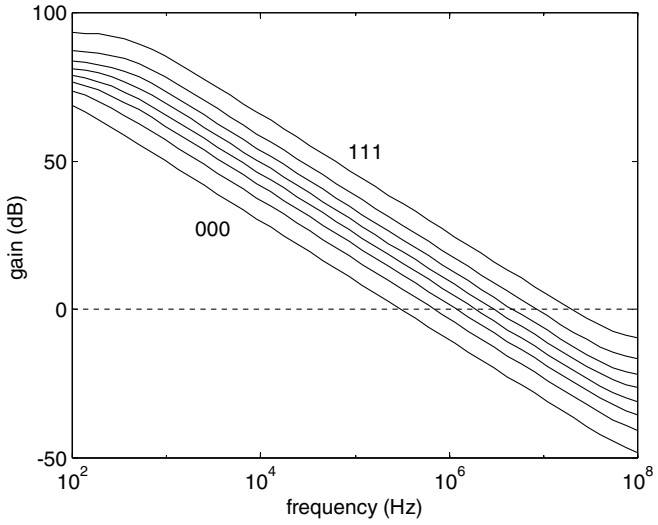

Fig. 3. Frequency response of the programmable integrator.

In order to reduce both short-channel and mismatch effects, the MOS transistors in the current divider are biased in the triode region and do not have minimal lengths. Resistor R is implemented with high resistivity polysilicon, to avoid introducing distortion into the system, and its value must be chosen so as to moderately load the OTA. Capacitors used are poly–poly.

The resolution in frequency of the programmable integrator is given by the word length n and the factor m. To show its feasibility, simulations were carried out for a 0.35 μm process in the CADENCE DFII environment using a Spectre simulator. Fig. 3 shows the frequency response of an integrator with $R_{in} = 6\,k\Omega$, $C_f = 10.6$ pF, $n = 3$ and $m = 1$. The resistive load of each OTA is always over 1 kΩ. The unity gain frequency varies almost linearly in a logarithmic scale, so it is suitable for continuous-time filters and sinusoidal oscillators requiring high frequency variation ranges. Furthermore, high linearity is achieved through the use of the MOS Current Divider.

Note that removing the output buffer from the active cell reduces its consumption. In fact, the total area and power dissipation of the programmable integrator are comparable to those of other single opamp implementations found in literature for the same technology [12].

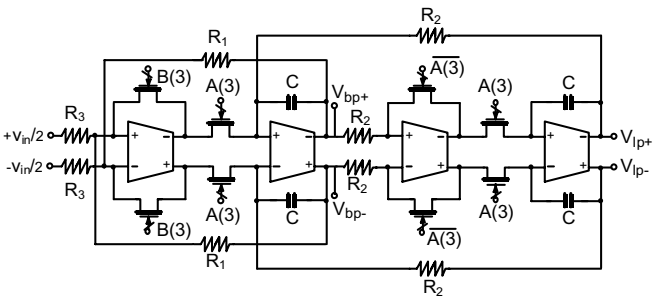

Fig. 4. Programmable biquad.

3. Programmable low-pass filter

The proposed low-pass filter is a 4th order Butterworth implementation. It is composed of two 3-bit programmable biquads like the one shown in Fig. 4.

The characteristic equations of the biquad are:

$$f_0 = \frac{1}{2\pi R_2 C}\left(\frac{\Delta_A}{1-\Delta_A}\right)^{1/2} \tag{3}$$

$$Q = \frac{R_1}{R_2}\left(\frac{\Delta_A}{1-\Delta_A}\right)^{1/2}\frac{(1+m_B D_Q)}{(1+m_A D_f)} \tag{4}$$

$$\left|\frac{v_{lp}}{v_{in}}\right| = \frac{R_2}{R_3}\frac{(1+m_A D_f)}{(1+m_B D_Q)} \tag{5}$$

$$\left|\frac{v_{bp}}{v_{in}}\right| = \frac{R_1}{R_3} \tag{6}$$

where

$$\Delta_A = \frac{1}{[m_A(2^n-1)+2]}(1+m_A D_f) \tag{7}$$

$$D_f = \sum_{j=0}^{n-1} a_j 2^j \tag{8}$$

$$D_Q = \sum_{j=0}^{n-1} b_j 2^j \tag{9}$$

The 4th order Butterworth filter is implemented by cascading two biquads with quality factors $Q_1 = 0.54$ and $Q_2 = 1.31$. For each frequency there is a specific word $D_Q(3)$ providing the appropriate value of both quality factors, as shown in Fig. 5.

Gain control without affecting linearity is provided by a highly linear programmable gain amplifier (PGA) [13] preceding each biquad. The whole system is shown in Fig. 6. It is worth noting that the same approach can be used for any kind of filter as long as it is based on an RC-active topology.

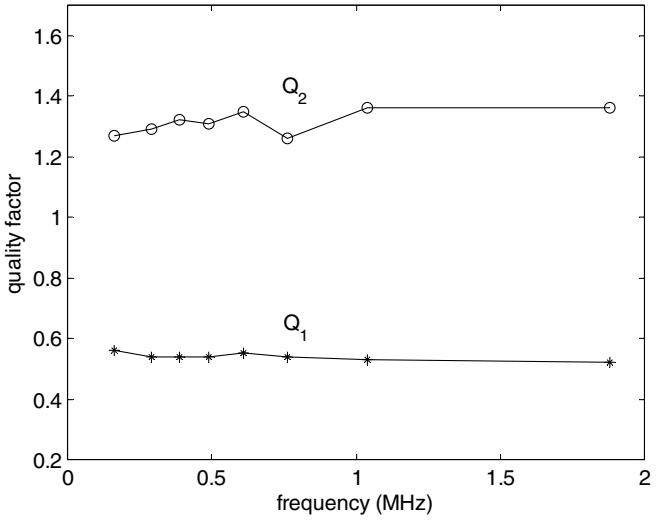

Fig. 5. Automatic control of Q_1 and Q_2 for each frequency setting.

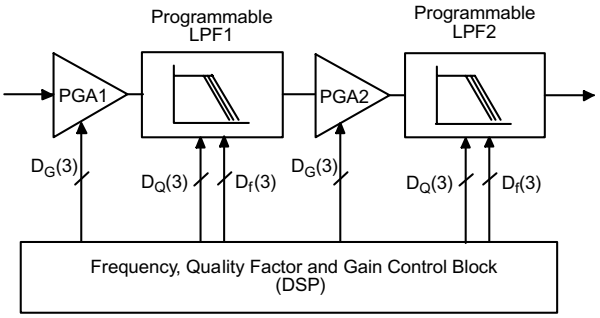

Fig. 6. Programmable 4th order butterworth filter.

4. Experimental results

To verify the former analysis, a 3-bit programmable low-pass filter was integrated in 0.35 μm technology and measurements were performed on the circuit for 2.5 V supply voltage. Detail of the chip is shown in Fig. 7.

For all measurements the filter was driven by a single-ended-to-balanced voltage converter and the differential output voltage was converted to a single output voltage. Both input and output converters were based on high performance AD844 current feedback opamps, which exhibit 60 MHz bandwidth and non-linear distortion lower than −86 dB.

Fig. 8 shows the characteristic frequency of the Butterworth filter for each digital word $D_f(3)$. The unity gain frequency varies almost linearly in a logarithmic scale for the central words and moves away from this tendency for the words {000} and {111}. This is due to the fact that, as already mentioned, (1) is not exactly an exponential function but an approximation to it.

Fig. 9 shows the frequency response for each control word $D_f(3)$ and Fig. 10 shows the gain setting for each word $D_G(3)$. As shown, tuning ranges of one decade in frequency and 39 dB in gain are obtained.

Distortion is mainly due to mismatches in the threshold voltage of the transistors which constitute the MOS

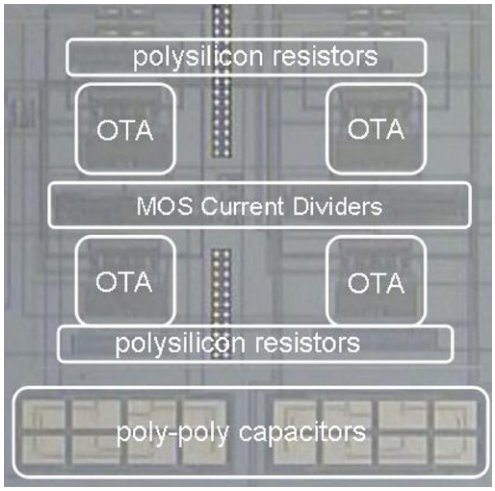

Fig. 7. Chip detail (biquadratic section).

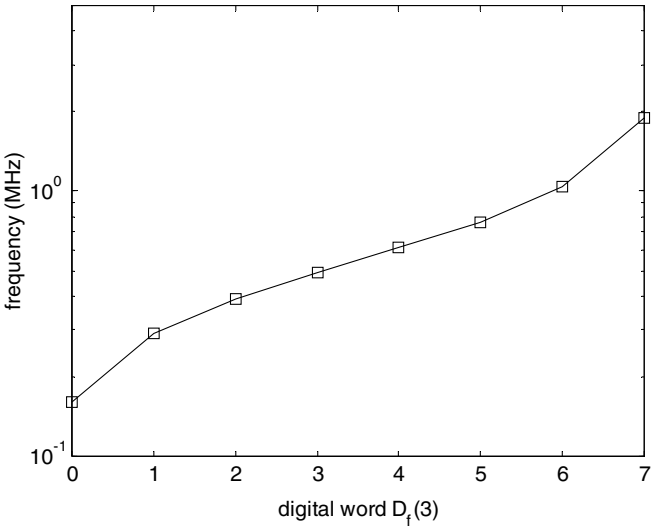

Fig. 8. Characteristic frequency of the filter for each word $D_f(3)$.

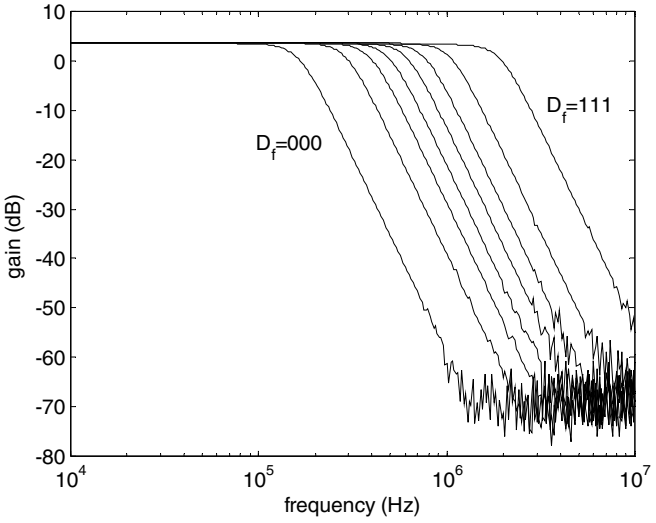

Fig. 9. Frequency response of the filter for each word $D_f(3)$.

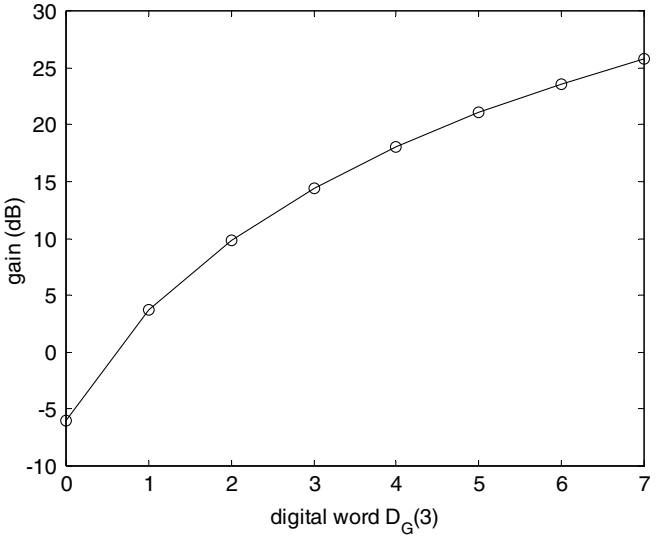

Fig. 10. Gain setting of the filter for each word $D_G(3)$.

Table 3
3-bit low-pass filters performance

Parameter	This work	Jussila [1]	Alzaher [14]	Nader [15]
Filter order and type	4th order butterworth	5th order Butterworth	6th order butterworth	5th order Butterworth
Technology	0.35 μm CMOS	0.35 μm BiCMOS	0.5 μm CMOS	0.25 μm BiCMOS
Supply voltage	2.5 V	2.7 V–3.0 V	2.7 V	2.5 V
Gain setting	−6–33 dB	−9–69 dB	18 dB	6 dB
Bandwidth	0.16–1.88 MHz	2/4/8 MHz	5 kHz–5 MHz	600 kHz/6 MHz
Area	0.11 mm^2	4.8 mm^2	1.25 mm^2	0.9 mm^2
Quiescent power	12 mW	21/25/38 mW	6 mW	2.25/6.75 mW
Distortion	THD[a] = −65 dB	IIP3 = +14 dBm IIP2 = +60 dBm	IIP3 = 61–51.4 dBm	IIP3 = 40 dBm
SNR@(THD = −65 dB)	59 dB	–	–	–

[a] (10 kHz@2$V_{p\text{-}p}$@gain > 0 dB).

Current Divider (see appendix). In the actual 0.35 μm process, a standard deviation of the threshold voltage $\sigma(\Delta Vt) = 4.7$ mV was reported by foundry for these transistors. The measured distortion level is better than −65 dB for a 10 kHz and 2 $V_{p\text{-}p}$ signal.

Table 3 shows the measured performance summary of the integrated circuit. The area and power consumption of the proposed filter is comparable to that of other systems employing simpler basic cells. In [1], for example, a 5th order Butterworth filter in 0.35 μm BiCMOS technology was presented. This consisted of operational amplifiers and banks of switchable resistors and capacitors. A comparison between that filter and the one proposed in this paper is shown in Table 3. The chip area in [1] is larger because of the area occupied by banks of programmable MIM capacitors and high ohmic polysilicon resistors. A wider frequency tuning range is obtained in our work with lower power consumption. Other recently published topologies are included in Table 3. Note that the proposed design takes up less silicon area and shows a wider gain setting for the same order of power consumption [14,15].

5. Conclusions

In this paper, an approach to designing highly linear CMOS programmable filters has been proposed that takes advantage of the inherently linear current division principle. Experimental results for a 3-bit 4th order Butterworth filter confirm the feasibility and good performance of the proposed technique. This programmable cell is suitable for use in analogue front-end for 10-bit accuracy digital systems fabricated in standard CMOS technologies.

Acknowledgement

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Appendix A

In order to show the high linearity of the proposed approach, the charge-sheet model [16] is employed. No approximate strong inversion models are used because they suffer from severe limitations when estimating distortion in MOS cells. The MOS Resistive Circuit [4,5], for example, shows no distortion when analysed with an approximate model in strong inversion. However, when the charge-sheet model is employed, distortion levels in the order of −50 dB for 1 $V_{p\text{-}p}$ output signal are obtained [17], which agrees with experimental results.

According to the charge-sheet model, the drain current in a long-channel MOS transistor is given by:

$$I_D = K[f(\psi_{sL}) - f(\psi_{s0})] \tag{10}$$

with

$$K = \mu C'_{ox}\frac{W}{L} \tag{11}$$

$$f(\psi_s) = f_1(\psi_s) + f_2(\psi_s) \tag{12}$$

where

$$f_1(\psi_s) = (V_{GB} - V_{FB})\psi_s - \frac{1}{2}\psi_s^2 - \frac{2}{3}\gamma\psi_s^{3/2} \tag{13}$$

$$f_2(\psi_s) = (\phi_t\psi_s + \phi_t\gamma\psi_s^{1/2}) \tag{14}$$

and where W and L are the channel width and length, μ is the carrier effective mobility, C'_{ox} is the gate oxide capacitance per unit area, V_{GB} is the gate to bulk voltage, V_{FB} is the flatband voltage, γ is the body effect parameter, ϕ_t is the thermal voltage and ψ_{s0} and ψ_{sL} are the source and drain surface potential, respectively. The function $f_1(\psi_s)$ corresponds to the drain current component due to drift and the function $f_2(\psi_s)$ to the drain current component due to diffusion.

In strong inversion the surface potentials can be defined as:

$$\psi_{s0} \approx V_{SB} + g(V_G, V) \tag{15}$$

$$\psi_{sL} \approx V_{DB} + g(V_G, V) \tag{16}$$

where $g(V_G, V)$ is a non-linear function of $V_G - V$. Furthermore, in strong inversion the current is almost totally due to drift. Thus, introducing (15) and (16) into (13) the drain current in the long-channel MOS transistor is obtained:

$$I_D = K[F(V_G, V_D) - F(V_G, V_S)] \tag{17}$$

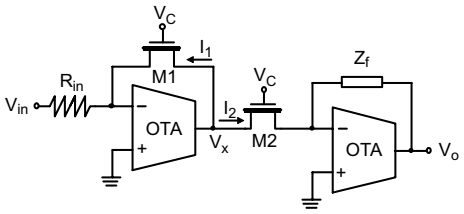

Fig. 11. MCD-based basic cell.

where

$$F(V_G, V_X) = (V_G - V_B - V_{FB})[V_X + g(V_G - V_X)] - \frac{1}{2}[V_X - V_B + g(V_G - V_X)]^2 - \frac{2}{3}\gamma[V_X - V_B + g(V_G - V_X)]^{3/2} \quad (18)$$

Fig. 11 shows the schematic of a basic cell made using two matched MOS transistors working as a MOS Current Divider (MCD). Assuming ideal OTAs, i.e., with infinite open-loop transconductance, the drain currents I_1 and I_2 in Fig. 11 are:

$$I_1 = K_1[F_1(V_C, V_X) - F_1(V_C, 0)] = -V_{in}/R_{in} \quad (19)$$

$$I_2 = K_2[F_2(V_C, V_X) - F_2(V_C, 0)] = -V_o/Z_f \quad (20)$$

If M_1 and M_2 are perfectly matched, $F_1(\cdot) = F_2(\cdot)$ and the transfer function of the cell is given by:

$$\frac{V_o}{V_{in}} = \frac{Z_f}{R_{in}}\frac{K_2}{K_1} = \frac{Z_f}{R_{in}}\frac{(W/L)_2}{(W/L)_1} \quad (21)$$

The dependence of V_X (or V_o) on V_{in} (or V_X) is not linear. However, Eq. (21) shows a linear dependence of the output signal V_o on the input signal V_{in} [10]. Mismatches in geometry, oxide thickness or mobility influence the accuracy of gain in the case of an MCD-based voltage amplifier ($Z_f = R_f$) or the accuracy of unity gain frequency in the case of an MCD-based integrator ($Z_f = C_f$), but do not affect the linearity of the output signal, as inferred from Eq. (21). If there are mismatches in other process parameters such as the body effect coefficient or the flatband voltage, $F_1(\cdot) \neq F_2(\cdot)$ and distortion arises.

Note that (21) shows an expected result. V_X is a complicated non linear function of V_{in}, $V_X = f(V_{in})$, whereas V_o is another complicated non linear function of V_X, $V_o = g(V_X)$. If transistors M_1 and M_2 are perfectly matched and their operating points are the same, $f(\cdot)$ is the inverse function of $g(\cdot)$, $f(\cdot) = g^{-1}(\cdot)$, except for a proportionality factor given by transistor sizes.

References

[1] Jussila J, Pärssinen A, Halonen K. An analog baseband circuitry for a WCDMA direct conversion receiver. Proceedings of European solid-state circuits conference (ESSCIRC'99) 1999:166–9.
[2] Marques LCC, Galup-Montoro C, Noceti Filho S, Schneider MC. A switched-MOSFET filter for application in hearing aid devices. Proceedings of the IEEE international symposium on circuits and systems (ISCAS'01) 2001:77–80.
[3] Tsividis Y, Banu M, Khoury J. Continuous-time MOSFET-C filters in VLSI. IEEE J Solid-State Circ 1986;21(1):15–30.
[4] Czarnul Z. Novel MOS resistive circuit for synthesis of fully integrated continuous-time filtres. IEEE Trans Circ Syst 1986;33(7):718–21.
[5] Song B-S. CMOS RF circuits for data communications applications. IEEE J Solid-State Circ 1986;21(2):310–7.
[6] Moon U-K, Song B-S. Design of a low-distortion 22-kHz fifth-order bessel filter. IEEE J Solid-State Circ 1993;28(12):1254–64.
[7] Vavelidis K, Tsividis Y. R-MOSFET structure based on current division. Electron Lett 1993;29(9):732–3.
[8] Durham AM, Redman-White W, Hughes JB. High-linearity continuous-time filter in 5-V VLSI CMOS. IEEE J Solid-State Circ 1992;27(9):1270–6.
[9] Alzaher HA, Ismail M. Digitally tuned analogue integrated filters using R–2R ladder. Electron Lett 2000;36(15):1278–80.
[10] Bult K, Geelen GJGM. An inherently linear and compact MOST-only current division technique. IEEE J Solid-State Circ 1992;27(12):1730–5.
[11] Razavi B. Design of analog CMOS integrated circuits. New York: McGraw-Hill; 2001.
[12] Chilakapati U, Fiez TS, Eshraghi A. A CMOS transconductor with 80-dB SFDR up to 10 MHz. IEEE J Solid-State Circ 2002;37(3):365–70.
[13] Sanz MT, Celma S, Calvo B. MOS current divider based PGA. Microelectron Reliabil 2005;45:727–32.
[14] Alzaher HA, Elwan HO, Ismail M. A CMOS highly linear channel-select filter for 3 G multistandard integrated wireless receivers. IEEE J Solid-State Circ 2002;37(1):27–37.
[15] Nader Mohieldin A, Sánchez-Sinencio E. A dual-mode low-pass filter for 802.11 b/bluetooth receiver. Proceedings of the 30th European solid-state circuits conference (ESSCIRC'04) 2004:423–6.
[16] Tsividis Y. Operation and modeling of the MOS transistor. 2nd ed. New York: McGrawHill; 1999.
[17] Flandre D, Jespers P. Charge-sheet modelling of MOS *I–V* fundamental nonlinearities in MOSFET-C continuous-time filters. Electron Lett 1995;31(17):1419–20.