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MOS current divider based PGA

M. Teresa Sanz *, Santiago Celma, Belén Calvo, Juan P. Alegre

Área de Electrónica, Departamento Ingeniería Electrónica y Comunicaciones, Facultad de Ciencias, Universidad de Zaragoza, Pedro Cerbuna 12, E-50009 Zaragoza, Spain

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Abstract

A highly linear, digitally programmable gain amplifier (PGA) based on an inherently linear MOS current divider (MCD) is presented in this paper. A 3-bit prototype with a total variation range of 36 dB in gain has been implemented in a 3.3 V–0.35 μm CMOS process with 2.5 V supply voltage. Experimental results prove the high linearity of the system, which presents distortion levels better than −70 dB for 1 MHz and 1 V_{p-p} output signals.

1. Introduction

The presence of a massive digital core in mixed analogue–digital systems results in many complications on the analogue side, such as crosstalk noise contamination of the sensitive analogue signals or voltage supply downscale related issues, among others. Nevertheless, the designer can take advantage of the digital circuitry in the chip to implement high accuracy automatic gain control of the variable gain amplifier and digital tuning of the analogue filter. Digital programmability is thus becoming an essential feature for complex mixed-signal systems. The built-in DSP is often used to accurately compute the control signal for the reconfiguration of the analogue side.

In all these applications, analogue pre-processing of the signal must offer at least the same accuracy as the associated A/D converters. In consequence, for applications over the baseband and telecommunication ranges, a dynamic range of at least 65 dB and linearity better than −70 dB are necessary.

Unfortunately, it is not easy to achieve this performance with fully integrated circuits in current CMOS technologies and it becomes even more difficult as the operating frequency increases and supply voltage reduces.

MOS resistive circuits [1–5] show distortion levels higher than −60 dB for 1 V_{p-p} signal swing in single 5 V systems. Furthermore, the tuning capability of this approach is extremely limited for low-voltage systems, as the mechanism of tuning is based on the variation of the gate voltage of transistors operating in the triode region.

For low voltage compatibility, a possible solution is to use programmable arrays of polysilicon resistors and/or capacitors [6]. High linearity and dynamic range have been achieved with this approach. Unfortunately, the maximum operating frequency is limited by the presence of MOS switches in the signal path. Furthermore, extensive area is needed to guarantee a minimum of accuracy [7].

* Corresponding author. Tel.: +34 976761240; fax: +34 976762143.
E-mail addresses: materesa@unizar.es (M.T. Sanz), scelma@unizar.es (S. Celma), becalvo@unizar.es (B. Calvo).

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In [8] a programmable gain amplifier (PGA) based on a degenerated differential pair with transconductance enhancement was presented. Even though a good linearity was achieved, its area and power consumption were high because of the use of an interpolated R–2R ladder and g_m-boosting amplifiers. A PGA based on a source-degenerated differential pair for higher frequency operation was proposed in [9]. Although lower distortion levels than those of similar approaches were achieved by using a linearization technique, linearity is limited by open-loop operation.

An approach combining good linearity and moderate area consumption is the use of MOS transistor configurations which make use of the inherently linear current division principle [10]. This is the case of the PGA presented in [11], where high linearity is achieved. However, the employed active cells limit bandwidth and increase area consumption.

This paper describes the principles, design and experimental results of a highly linear PGA in standard CMOS technology for the low megahertz range. In Section 2 the principle of operation of the PGA, which is based on the inherently linear current division principle, is explained. In order to show the high linearity of the proposed approach, the charge-sheet model [12] is employed. No approximate strong inversion models are used because they suffer from severe limitations when estimating distortion in MOS cells. The MOS resistive circuit [2,3], for example, shows no distortion when analysed with an approximate model in strong inversion. However, when the charge-sheet model is employed, distortion levels in the order of −50 dB for $1\,V_{p-p}$ output signal are obtained [13], which agrees with experimental results.

Section 3 describes the proposed PGA. Experimental results are discussed in Section 4 and some conclusions are drawn in Section 5.

2. Principle of operation

According to the charge-sheet model, the drain current in a long-channel MOS transistor is given by

$$I_D = K[f(\psi_{sL}) - f(\psi_{s0})] \tag{1}$$

with

$$K = \mu C'_{ox}\frac{W}{L} \tag{2}$$

$$f(\psi_s) = f_1(\psi_s) + f_2(\psi_s) \tag{3}$$

where

$$f_1(\psi_s) = (V_{GB} - V_{FB})\psi_s - \frac{1}{2}\psi_s^2 - \frac{2}{3}\gamma\psi_s^{3/2} \tag{4}$$

$$f_2(\psi_s) = (\phi_t\psi_s + \phi_t\gamma\psi_s^{1/2}) \tag{5}$$

and where W and L are the channel width and length, μ is the carrier effective mobility, C'_{ox} is the gate oxide capacitance per unit area, V_{GB} is the gate to bulk voltage, V_{FB} is the flatband voltage, γ is the body effect parameter, ϕ_t is the thermal voltage and ψ_{s0} and ψ_{sL} are the source and drain surface potential, respectively. The function $f_1(\psi_s)$ corresponds to the drain current component due to drift and the function $f_2(\psi_s)$ to the drain current component due to diffusion.

In strong inversion the surface potentials can be defined as:

$$\psi_{s0} \approx V_{SB} + g(V_G, V) \tag{6}$$

$$\psi_{sL} \approx V_{DB} + g(V_G, V) \tag{7}$$

where $g(V_G,V)$ is a non-linear function of $V_G - V$. Furthermore, in strong inversion the current is almost totally due to drift. Thus, introducing (6) and (7) into (4) the drain current in the long-channel MOS transistor is obtained:

$$I_D = K[F(V_G, V_D) - F(V_G, V_S)] \tag{8}$$

where

$$F(V_G, V_X) = (V_G - V_B - V_{FB})[V_X + g(V_G - V_X)] - \frac{1}{2}[V_X - V_B + g(V_G - V_X)]^2 - \frac{2}{3}\gamma[V_X - V_B + g(V_G - V_X)]^{3/2} \tag{9}$$

Fig. 1 shows the schematic of a voltage amplifier made using two matched MOS transistors working as a MOS current divider (MCD). Assuming ideal OTAs, i.e., with infinite open-loop transconductance, the drain currents I_1 and I_2 in Fig. 1 are:

$$I_1 = K_1[F_1(V_C, V_x) - F_1(V_C, 0)] = -V_{in}/R_1 \tag{10}$$

$$I_2 = K_2[F_2(V_C, V_x) - F_2(V_C, 0)] = -V_o/R_2 \tag{11}$$

If M_1 and M_2 are perfectly matched, $F_1(\cdot) = F_2(\cdot)$ and the transfer function of the amplifier is given by

$$\frac{V_o}{V_{in}} = \frac{R_2}{R_1}\frac{K_2}{K_1} = \frac{R_2}{R_1}\frac{(W/L)_2}{(W/L)_1} \tag{12}$$

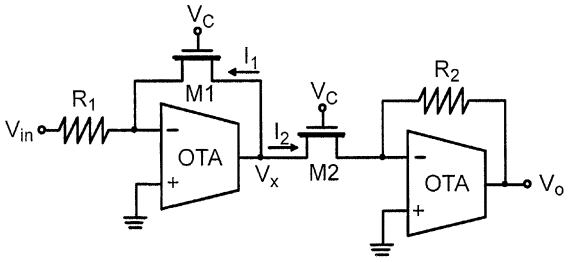

Fig. 1. MCD based voltage amplifier.

The dependence of V_x (or V_o) on V_{in} (or V_x) is not linear. However, Eq. (12) shows a linear dependence of the output signal V_o on the input signal V_{in} [10]. Mismatches in geometry, oxide thickness or mobility influence the accuracy of the gain but do not affect the linearity of the signal in the MCD based voltage amplifier, as inferred from Eq. (12). If there are mismatches in other process parameters such as the body effect coefficient or the flatband voltage, $F_1(\cdot) \neq F_2(\cdot)$ and distortion arises.

Note that (12) shows an expected result. V_x is a complicated non-linear function of V_{in}, $V_x = f(V_{in})$, whereas V_o is another complicated non-linear function of V_x, $V_o = g(V_x)$. If transistors M_1 and M_2 are perfectly matched and their operating points are the same, $f(\cdot)$ is the inverse function of $g(\cdot)$, $f(\cdot) = g^{-1}(\cdot)$, except for a proportionality factor. This proportionality factor is the linear gain as expressed in (12).

3. MCD based PGA

Fig. 2 shows the proposed fully balanced PGA making use of the MCD. In order to reduce both short-channel and mismatch effects, the MOS transistors are biased in the triode region and do not have minimal lengths. We propose the use of wide-band OTAs and banks of MOS transistors in parallel. In this way, the bandwidth can be expanded beyond that of PGAs based on R–2R networks and opamps [14,15]. Complementary words are applied to identical n-bit programmable transistor banks with binary weighted transistor sizes. The differential output voltage $V_o = V_o^+ - V_o^-$ can be expressed as:

$$\frac{V_o}{V_{in}} = \frac{\Delta}{1-\Delta}\frac{R_2}{R_1}\eta$$

$$\text{with } \Delta = \frac{1}{[m(2^n-1)+2]}\left(1 + m\sum_{j=0}^{n-1} a_j 2^j\right) \qquad (13)$$

Factor η appears as a result of the influence of the finite OTA transconductance value G_m. If G_m is in the order of 100 mA/V for an equivalent load resistance $R_L = 10\,k\Omega$, then $\eta = 0.99$, that is, the OTA works as a wide-band operational amplifier with an error in gain of 1%. A high transconductance two-stage OTA with resistor-driving capability has been specifically designed as shown in Fig. 3. Although not shown in the figure, a CMFB circuit and a supply independent biasing circuit have been used [16].

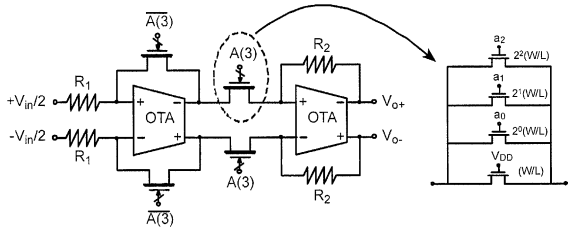

Fig. 2. Three-bit programmable gain amplifier. $A(3) = \{a_2\ a_1\ a_0\}$, $\overline{A}(3) = \{\bar{a}_2\ \bar{a}_1\ \bar{a}_0\}$, $a_i \in \{0, V_{DD}\}$.

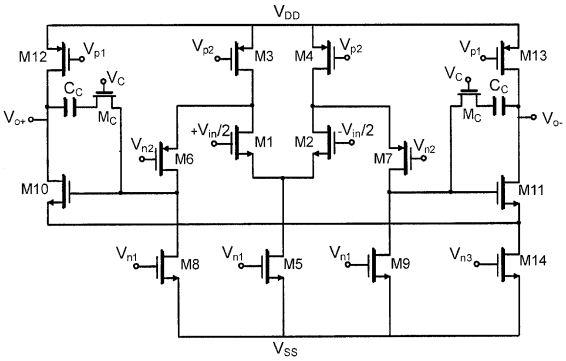

Fig. 3. Scheme of the fully-differential OTA (CMFB circuit omitted).

The gain setting resolution of the PGA is given by the word length n and the factor m, which is the size ratio between transistors M_{a0} and M_a, i.e., $m = (W/L)_{a0}/(W/L)_a$.

Note that the voltage gain given by (13) is approximately exponential for the central word values. For instance, for a total variation range of 36 dB ($m = 1$, $n = 3$, $R_2/R_1 = 3$) the gain increases linearly on a dB-scale over a 20 dB range with a maximum gain deviation from exponential behaviour of 0.36 dB. Outside the central region the rate of change in gain is even faster, which provides even better control of the output voltage in comparison to a simple exponential gain characteristic [17]. The PGA is thus characterized by its inherently high linearity and wide range in gain, which can be digitally programmed without affecting the dynamic range and THD. Resistors R_1 and R_2 are implemented with high resistivity polysilicon and their values must be chosen so as to moderately load the OTA.

4. Experimental results

To verify the former analysis, a 3-bit PGA with $m = 1$ was integrated in 0.35 μm technology and measurements were performed on the circuit. Detail of the chip is shown in Fig. 4.

For all measurements the PGA was driven by a single-ended-to-balanced voltage converter and the differential output voltage was converted to a single output voltage. Both input and output converters were based on high performance AD844 current feedback opamps, which exhibit 60 MHz bandwidth and non-linear distortion lower than −86 dB. Distortion measurements at

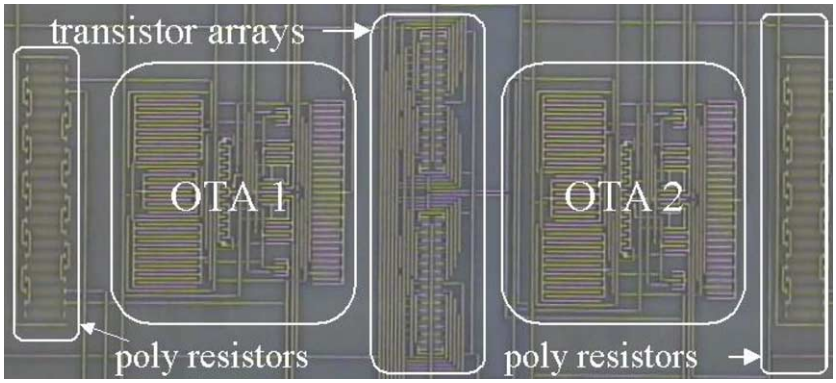

Fig. 4. Chip microphotograph (90 μm × 280 μm).

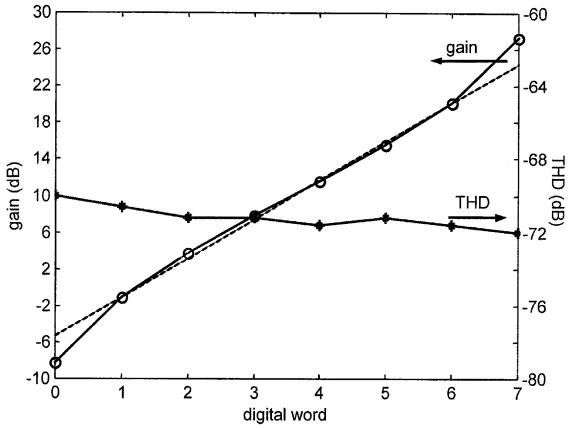

Fig. 5. (○) Gain setting ($n = 3$, $m = 1$, $R_f/R_l = 3$) and (⁎) THD (1 MHz @ 1 V_{p-p} output signal) for each control word.

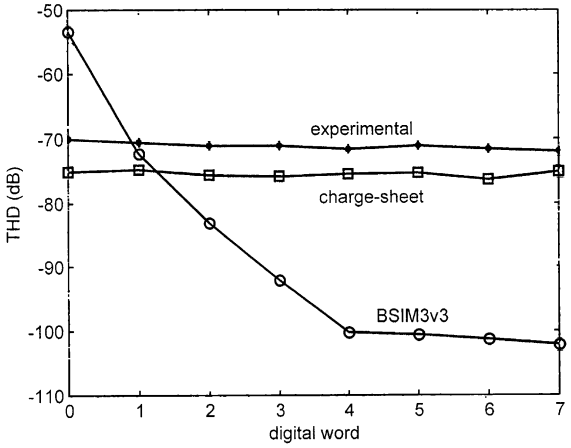

Fig. 6. (⁎)Experimental THD (1 MHz @ 1 V_{p-p} output signal) for each gain setting and simulated results with (○) the BSIM3v3 and (□) the *charge-sheet* model.

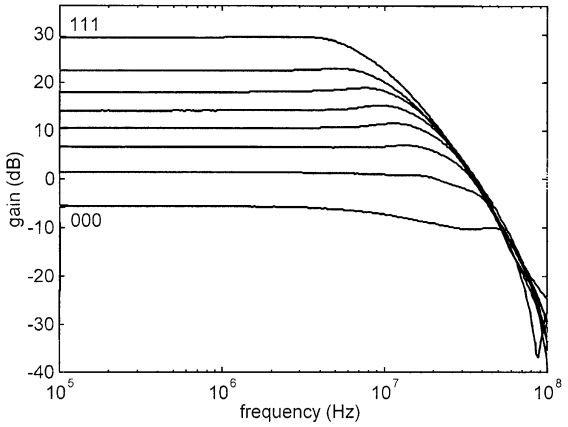

Fig. 7. Frequency response for each gain setting ($n = 3$, $m = 1$, $R_f/R_l = 3$).

1 MHz were challenging, as test signals provided by the signal generator showed higher residual distortion than those meant to be measured. A simple technique for high frequency low distortion measurements was employed [18].

Table 1
Three-bit PGA performance

Parameter	Value
CMOS technology	0.35 μm
Supply voltage	2.5 V
Gain setting	−8 to 28 dB
Maximum gain error	0.27 dB
Bandwidth	16 MHz
Area	0.025 mm^2
Quiescent power	8 mW
Settling time (1–99%)	30 ns
THD (1 MHz @ 1 V_{p-p} output)	−70 dB
Input referred noise @ {1 1 1}	50 nV/$\sqrt{Hz}$

Table 2
Performance comparison of PGAs

	Rijns [8]	Elwan et al. [11]	Calvo et al. [9]	This work
CMOS technology (μm)	0.8	1.2	0.35	0.35
Supply voltage (V)	5.0	3.2	3.3	2.5
Gain range (dB)	14 (3 bits)	25 (6 bits)	16 (3 bits)	36 (3 bits)
Bandwidth (MHz)	15	4.1	250	16
THD (dB)	−65[a]	−68[b]	−60[c]	−70[a]
Quiescent power (mW)	25	2.3	1.95	8
Area (mm^2)	0.175	0.442	0.010	0.025

[a] 1 MHz @ 1 V_{p-p} differential output signal.
[b] Conditions not specified.
[c] 100 kHz @ 0.4 V_{p-p} differential output signal.

Fig. 5 shows the gain setting and THD (1 MHz @ 1 V_{p-p} output signal) of the PGA for each digital word. It can be seen that dB-gains are approximately equally spaced for the central words and move away from this tendency for the words {000} and {111}. This is due to the fact that, as already mentioned, (12) is not exactly an exponential function but an approximation to it. The linearity of the whole system remains very high over the whole amplification range, as distortion levels obtained are better than −70 dB for a 1 MHz and 1 V_{p-p} output signal for every gain.

As explained in Section 2, distortion is mainly due to mismatches in the threshold voltage of the transistors which constitute the MCD. In the actual 0.35 μm process, a standard deviation of the threshold voltage $\sigma(\Delta V_t) = 4.7$ mV was reported by foundry for these transistors. Fig. 6 shows the simulated THD (1 MHz @ 1 V_{p-p} output signal) for each gain setting considering the given $\sigma(\Delta V_t)$ and employing both the BSIM3v3 model provided in the design kit of the technology and the *charge-sheet* model. It is shown that the BSIM3v3 model does not fit in with experimental results. The charge-sheet model, on the contrary, fairly approaches the measured results.

The standard deviation of factor K, $\sigma(\Delta K/K) = 0.4\%$, only affects gain accuracy. A maximum gain error of 0.27 dB was measured.

Fig. 7 shows the frequency response for each word. Table 1 shows the measured performance summary of the integrated circuit. In Table 2 the performance of the proposed PGA is compared to three previous realizations in CMOS technology [8,9,11]. It is worth noting that the MOS Current Divider based PGA achieves the lowest distortion level. It also shows the best trade-off between bandwidth, non-linear distortion and power consumption.

5. Conclusions

In this paper, an approach to designing highly linear CMOS PGAs has been proposed that takes advantage of the inherently linear current division principle. Experimental results for a 3-bit PGA confirm the feasibility and good performance of the proposed technique. A dynamic range better than 65 dB is achieved, so these programmable cells are suitable for use in analogue front-end (AGC and filtering) for 10-bit accuracy digital systems fabricated in standard CMOS technologies.

Acknowledgement

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