Self-cascode SOI versus graded-channel SOI MOS transistors

M.T. Sanz, S. Celma, B. Calvo and D. Flandre

Abstract: Two strategies to enhance transistor performance in SOI technology without increasing the operating voltage are compared. The first option is the use of the self-cascode transistor, a series connection of two conventional FD SOI MOSFETs which, with an appropriate choice of sizes, work as a single transistor with reduced output conductance. The second option is the use of the graded-channel (GC) SOI MOSFET, consisting of a modification of the fully-depleted (FD) SOI MOSFET which leads to better performance of the device in saturation. The paper shows the existing analogy between the operation of self-cascode and GC SOI transistors. The comparison between both strategies is carried out on the basis of simulations with the University of Florida SOI (UFSOI) model and experimental measurements. The area consumed by a self-cascode SOI transistor is estimated to be 10 times larger than that of a GC SOI transistor for the same improvement in output conductance. Experimental results validate the model used for the GC SOI device and also provide numerical quantification of output resistance increase in both configurations.

1 Introduction

The tendency towards a reduction of the supply voltage and transistor sizes over recent years has made it unfeasible to enhance analogue circuit performance by means of many of the traditionally employed techniques, such as the use of long channel transistors or conventional cascode structures.

The self-cascode configuration consists of two transistors connected in series working as a single transistor [1]. If sizes are appropriately chosen, the DC characteristic of the composite transistor is the same as that of a single transistor with a longer channel. Thus, a higher output impedance is obtained without detriment to voltage headroom. Section 2 explains this structure in more detail.

The second way of improving transistor performance presented in this paper is the use of a modified FD SOI transistor structure. When the devices are scaled down, premature breakdown and hot carrier effects occur. Several specialised transistor structures have been developed in bulk MOS as well as in FD SOI technology in order to reduce these effects [2]. The most common one is the lightly doped drain (LDD) structure, which reduces the peak electric field by spreading the drain voltage drop over a wider depletion region. This is accomplished by using a lower dose and by grading the impurity profile.

The GC SOI MOSFET is a newly introduced modified transistor with an asymmetrically doped channel region [3, 4]. It has shown to effectively increase the drain output resistance and the drain breakdown voltage as a result of the peak electric field reduction near the drain. The internal structure of the transistor, how it works, its fabrication process and the modelling of the device are explained in Section 3.

As will be shown, the GC SOI transistor can be modelled as the series connection of two FD SOI transistors with different characteristics. Thus, an analogy between the structure of self-cascode and GC SOI devices is drawn. Furthermore, both approaches provide better output characteristics than conventional MOSFETs at the expense of some increase in area consumption. They are used in simple sections of analogue circuits, especially when high-frequency and low-voltage operation are required. Several examples can be found in the literature: current mirrors [5–7], operational transconductance amplifiers [8], active loads [9, 10] etc.

A comparison between both techniques in terms of output characteristics, area consumption and frequency performance will be carried out in this paper to highlight the pros and cons of each configuration. Section 4 shows and compares the DC characteristics of single FD SOI MOSFETs, self-cascode devices with different size ratios and GC SOI transistors according to simulations. In Section 5 experimental measurements show the validity of the employed models and provide definitive results. Conclusions are drawn in Section 6.

2 Self-cascode MOSFETs

A self-cascode structure consists of two transistors in series as shown in Fig. 1. The transistor near the source of the equivalent composite transistor, M1, always operates in the non-saturation region, that is, it works as an independent resistor. For optimal operation, and supposing the lengths of M1 and M2 to be equal, M2 should be m times wider than M1, with m as high as possible. It can be demonstrated that the 'DC equivalent' electrical width of the composite transistor is equal to M2's width W_D, while the 'DC

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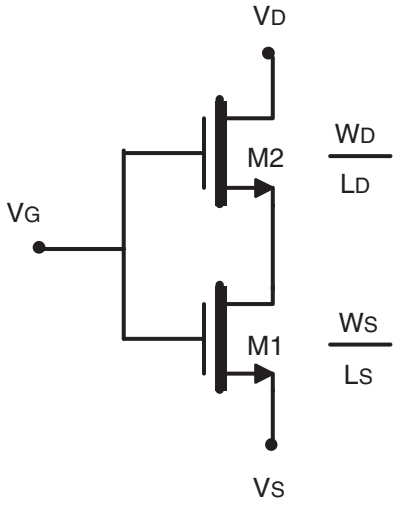

Fig. 1 *Self-cascode transistor*

equivalent' electrical length of the composite transistor equals $L_D + mL_S$. Therefore, for $m > 1$, a composite transistor equivalent to a long-channel transistor is obtained.

The output resistance of the equivalent transistor is given by

$$r_{o,eq} \approx (m+1) r_{o,D} \tag{1}$$

where $r_{o,D}$ is the output resistance of M2 (see Appendix).

Alternatively, the value of V_{DS} at onset of saturation is given by

$$V_{DS(sat),eq} \approx V_{GS} - V_{th} \tag{2}$$

A self-cascode structure thus offers high output impedance with output voltage requirements similar to those of a single transistor [11]. Note that the widths of M1 and M2 must be adequately enlarged to maintain the drive current.

When compared to its DC equivalent long-channel transistor, not only does the self-cascode device provide the same output resistance consuming m times less area. It also has a higher cut-off frequency as its physical channel length is shorter [1]. The configuration is therefore suitable for high-frequency, low-voltage analogue sections.

3 Graded-channel SOI MOSFETs

Although the advantages of SOI CMOS over bulk CMOS technology are widely known, the inherent parasitic bipolar effect in SOI remains a problem to overcome. It results in hysteresis, instability during dynamic operation, abnormal subthreshold slope and breakdown voltage degradation. Furthermore, as the device dimensions shrink, reliability problems appear owing to hot electron degradation, analogue performance worsens due to Early voltage lowering and threshold voltage decreases with the channel length. These effects can be reduced by using transistor structures with specially designed drain or channel regions [2, 12–14].

The GC SOI MOSFET is an asymmetric channel device which was recently introduced with the purpose of reducing the parasitic bipolar effects in SOI MOSFETs and improving their output characteristics. Conventional threshold voltage implantation is performed only for the region of the channel near the source, while the part of the channel near the drain, of length L_{LD}, is kept at natural wafer doping (Fig. 2). Through this reduction in the doping level, the impact ionisation is efficiently reduced and, as a result, the breakdown voltage is increased. The low-doped region

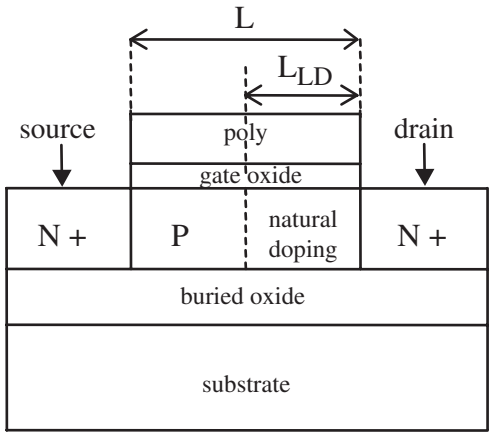

Fig. 2 *Cross-section of the GC SOI nMOSFET*

of the channel presents negative threshold voltage and can thus be interpreted as an extension of the drain region. The effective channel length of the device is therefore reduced to $L_{eff} = L - L_{LD}$, where L is the mask channel length and L_{LD} is the length of the low-doped region. These transistors showed significantly enhanced drain breakdown voltage, superior transconductance in saturation and reduced drain output conductance [3].

GC SOI nMOSFETs are processed in the same p-type Smartcut wafers as conventional FD SOI nMOSFETs, with an initial silicon film concentration of about $10^{15}\,cm^{-3}$. An additional photolithographic step is needed when fabricating GC SOI nMOSFETs in order to preserve the natural wafer doping near the drain while threshold voltage ionic implantation is performed near the source. However, this additional step can be suppressed in a full CMOS processing, as the same mask protecting the p-type devices from the n-type V_{th}-implant is used to mask the GC region.

GC transistors can be modelled as a series association of two conventional FD SOI MOSFETs with different characteristics, each FD transistor representing a part of the GC MOSFET channel region (Fig. 3). As the channel region near the drain is kept at natural wafer doping, that is, $N_{af,LD} = 10^{15}\,cm^{-3}$, the FD SOI transistor corresponding to this lightly doped region of the channel, M2, presents a negative threshold voltage, ($V_{th,LD} = -0.2\,V$) and higher mobility ($\mu_{LD} = 660\,cm^2/Vs$) than the conventionally doped region of the channel ($N_{af,HD} = 10^{17}\,cm^{-3}$). This channel region near the source, represented by M1, presents lower mobility ($\mu_{HD} = 450\,cm^2/Vs$) and its threshold voltage, $V_{th,HD} = 0.41\,V$, determines the threshold voltage of the GC transistor.

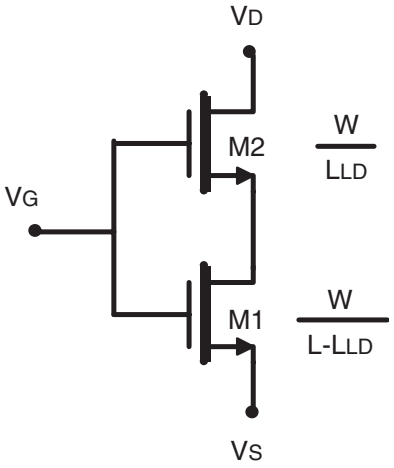

Fig. 3 *GC SOI transistor model*

There is a clear analogy between this model and the self-cascode structure. Note that if an SOI process with two different threshold voltages was available, the output impedance of a self-cascode transistor would be improved by choosing $V_{th,1} > V_{th,2}$ [11].

An analytical continuous model for long-channel GC SOI nMOSFETs was presented and validated in [15].

4 Simulation results

Simulations were carried out in the CADENCE DFII environment using a Spice simulator. The UFSOI model, a physical and process-based FD SOI model developed at the University of Florida, was employed. It considers parameters directly estimated from the device structure in addition to the pertinent device physics [16].

Simulation of a self-cascode transistor is straightforward. As for the GC SOI, it is modelled, as mentioned above, as a series connection of two transistors with different intrinsic parameters. In both the self-cascode and the GC SOI transistors, drain and source terminals cannot be interchanged, as they are physically different.

Figure 4 shows the DC characteristics of a FD SOI transistor with $W/L = 5\mu/2\mu$ and $W/L = 10\mu/4\mu$, a GC SOI transistor with $W = 5\,\mu m$, drawn length $L = 4\,\mu m$ and effective length $L_{eff} = 2\,\mu m$, and a self-cascode with $W_D/L_D = 15\mu/2\mu$ and $W_S/L_S = 7.5\mu/2\mu$ ($L_{drawn} = L_S + L_D = 4\,\mu m$; $m = 2$).

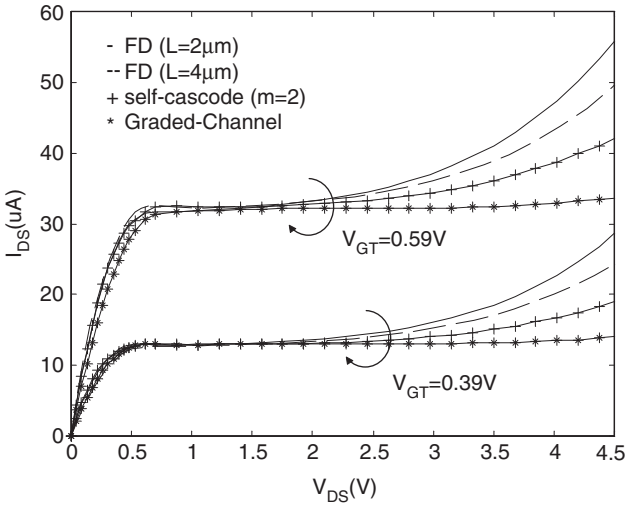

Fig. 4 *Simulated I_{DS} against V_{DS} for FD ($L = 2\,\mu m$ and $L = 4\,\mu m$), self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2$) and GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$)*

The reduction of the output conductance achieved with both strategies when compared to the output conductance of an equivalent single transistor can be appreciated in Fig. 4. Simulations have been made for different overdrive voltages ($V_{GT} = V_{GS} - V_{th}$). It is worth noting that the threshold voltage, V_{th}, is the same for the FD, self-cascode and GC SOI transistors, as the same V_{th}-implant is used in their fabrication ($V_{th} = 0.41\,V$).

Table 1 shows the output resistance for different drain-to-source voltages at $V_{GT} = 0.39\,V$. A drastic increase in the output resistance is attained by the GC SOI. Although to a lesser extent, the output resistance of the self-cascode also increases, substantially improving the output characteristics of the device. Table 2 shows the output resistance of a self-cascode transistor with drawn length $L_{drawn} = 4\,\mu m$ for different m values and drain to source voltages at $V_{GT} = 0.39\,V$.

Table 1: Comparison of output resistance obtained by simulation at $V_{GT} = 0.39\,V$ for FD ($L = 2\,\mu m$ and $L = 4\,\mu m$), GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$) and self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2$)

	Output resistance (kΩ)			
V_{DS} (V)	FD SOI ($L = 2\,\mu m$)	FD SOI ($L = 4\,\mu m$)	GC SOI ($L_{eff} = 2\,\mu m$)	SC SOI ($m = 2$)
1.5	814	814	5800	3500
2.5	227	312	11700	555
3.5	95	155	1600	206

Table 2: Self-cascode ($L_D = L_S = 2\,\mu m$) output resistance obtained by simulation for several m values at $V_{GT} = 0.39\,V$

	Self-cascode output resistance (kΩ)		
V_{DS} (V)	$m = 5$	$m = 10$	$m = 20$
1.5	5590	8839	15618
2.5	888	1400	2480
3.5	329	518	918

The GC SOI transistor not only provides lower output conductance, it also consumes less area than the FD and self-cascode SOI counterparts. Consider a single FD SOI MOSFET with width W_u, length L_u and area $A_u = W_u L_u$. A GC SOI transistor with the same drawn length L_u, provided that $L_{LD} = L_u/2$, must be $W_u/2$ wide to keep the same drive current. Its area is therefore $A_{GC} = L_u W_u/2$. In the case of a self-cascode transistor, if dimensions of the transistor near the source are $W_u/(L_u/2)$, the width of the transistor near the drain must then be $W_D = mW_u$ for the same length $L_u/2$. Note that the total drawn length is L_u, as for the FD and GC, whereas the total area consumed by the configuration is $A_{SC} = (1+m)W_u L_u/2$. According to simulations, to achieve the same improvement when employing self-cascode as when using GC SOI devices, m about 20 is required. Thus, the area consumed by the self-cascode transistor is more than 20 times larger than that necessary for a GC SOI, and over 10 times larger compared to the original single transistor. To achieve the same output conductance as the self-cascode, a single long-channel transistor requires $W = mW_u$ and $L = (1+m)L_u/2$, occupying m times more area than the self-cascode, as already mentioned in Section 2.

Regarding frequency behaviour, in [7] it was demonstrated, through two-dimensional process simulations, that the total intrinsic gate capacitance is similar in GC and FD SOI transistors. Thus, the GC configuration will not result in bandwidth degradation. For the self-cascode structure, on the contrary, the increase in the drain side transistor width increases the parasitic capacitances and thus degrades frequency performance.

5 Experimental results

The DC characteristics of integrated SOI transistors with $W/L = 10\mu/4\mu$ and GC SOI transistors with $W/L = 5\mu/4\mu$ and $L_{eff} = 2\,\mu m$ were measured and compared, as shown in Fig. 5, for two different overdrive voltage values. Then, connections of two FD SOI transistors in series, that is, self-cascode transistors, were measured. Figure 5 shows the experimental results for a self-cascode with $W_D/L_D = 18\mu/2\mu$

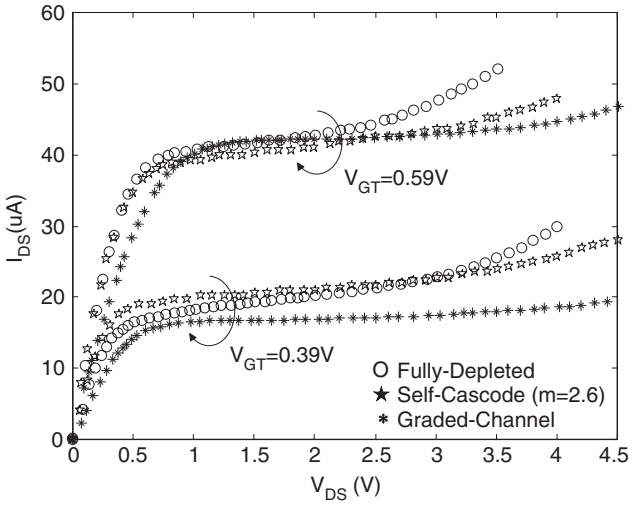

Fig. 5 *Measured I_{DS} against V_{DS} for FD ($L = 4\,\mu m$), self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2.6$) and GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$)*

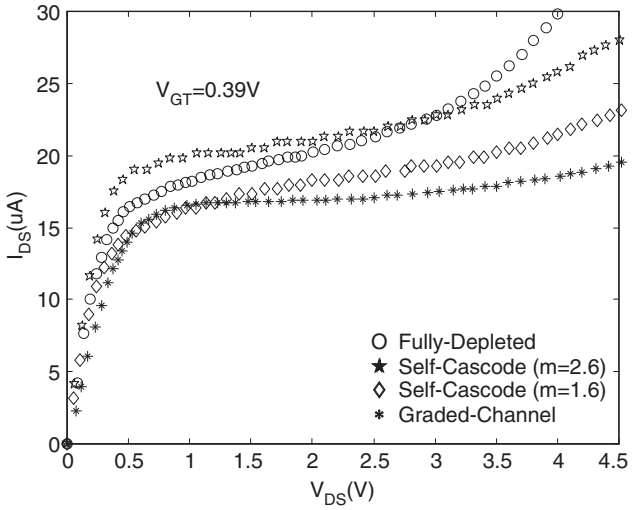

Fig. 6 *Measured I_{DS} against V_{DS} for FD ($L = 4\,\mu m$), self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2.6$ and $m = 1.6$) and GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$)*

and $W_S/L_S = 7\mu/2\mu$, that is, with a drawn length $L_{drawn} = 4\,\mu m$ and $m = 2.6$.

Measurements of a self-cascode with $W_D/L_D = 13\mu/2\mu$ and $W_S/L_S = 8\mu/2\mu$, ($L_{drawn} = 4\,\mu m$ and $m = 1.6$) were also made. Experimental results of the four considered cases at $V_{GT} = 0.39\,V$ are shown in Fig. 6.

Table 3 shows the output resistance extracted at different drain to source voltages for a FD and a GC SOI transistor, in addition to self-cascode transistors with different size ratios ($m = 1.67$ and 2.67), at $V_{GT} = 0.39\,V$.

Experimental output resistances are not as high as those provided by simulations, but the same conclusions can be drawn: the improvement of the device characteristics is notable for the self-cascode and outstanding for the GC SOI transistor. As experimental results show, short-channel effects are reduced for both the self-cascode configuration and the GC transistor. High V_{DS} values were considered to highlight their reduction. Note that short-channel effects are caused by the increase in the longitudinal electric field, i.e., they depend on V_{DS}/L; then, for a long channel technology short-channel effects can be reproduced in a good approximation by increasing V_{DS}.

Experimental results also validate the model employed for the simulation of GC SOI MOSFETs. It is thus possible to employ conventional simulation tools in the design of circuits using these modified devices.

Table 3: Comparison of experimental output resistance at $V_{GT} = 0.39\,V$ for FD ($L = 2\,\mu m$ and $L = 4\,\mu m$), GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$) and self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2.6$ and $m = 1.6$)

	Output resistance (kΩ)				
V_{DS} (V)	FD SOI ($L = 2\,\mu m$)	FD SOI ($L = 4\,\mu m$)	GC SOI ($L_{eff} = 2\,\mu m$)	SC SOI ($m = 2.6$)	SC SOI ($m = 1.6$)
1.0	308	560	800	400	1000
1.5	400	700	4000	666	570
2.0	286	460	4000	1300	1000
2.5	148	530	2000	1300	1000
3.0	111	400	1000	1300	570
3.5	–	188	800	666	364
4.0	–	134	800	308	210

Table 4: Experimental transition frequency at $V_{GT} = 0.39\,V$ for FD ($L = 2\,\mu m$ and $L = 4\,\mu m$), GC SOI ($L = 4\,\mu m$; $L_{eff} = 2\,\mu m$) and self-cascode ($L_D = L_S = 2\,\mu m$; $m = 2.6$ and $m = 1.6$)

Transition frequency f_T (GHz)				
FD SOI ($L = 2\,\mu m$)	FD SOI ($L = 4\,\mu m$)	GC SOI ($L_{eff} = 2\,\mu m$)	SC SOI ($m = 2.6$)	SC SOI ($m = 1.6$)
1.81	0.52	1.33	0.53	0.49

Finally, Table 4 shows the measured transition frequency of the transistors. The GC device shows the best frequency performance, whereas the self-cascode configuration has a similar transition frequency than the FD SOI. Thus, the suitability of both GC and self-cascode devices for high frequency applications is confirmed.

6 Conclusions

A comparison between single FD SOI, GC SOI and self-cascode SOI transistor performance was carried out. Both the GC and the self-cascode strategies have shown to enhance the transistor characteristics by reducing the output conductance and increasing the breakdown voltage. The advantage of self-cascode transistors is that remarkable enhancement is obtained with available conventional technology. However, the use of these transistors can drastically increase the area consumed by the circuit. Alternatively, the area consumed by a GC SOI transistor is estimated to be 10 times smaller than that of a self-cascode transistor with the same improvement in output conductance. Enhancement provided by a GC SOI transistor is far larger with even less area consumption and higher transition frequency than a FD SOI MOSFET with the same drawn length.

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9 Appendix

The equivalent output resistance and transconductance of the self-cascode configuration working in saturation are deduced in this appendix. As mentioned in Section 2, the transistor near the source of the equivalent composite transistor, M1, always operates in the non-saturation region. Thus, the transconductance $g_{m,D}$ of M2 (saturation) and the equivalent resistence $r_{o,S}$ of M1 (triode) are

$$g_{m,D} = \mu C_{ox} \frac{W_D}{L_D} (V_{GX} - V_{th}) \tag{3}$$

$$r_{o,S} = \frac{1}{\mu C_{ox} (W_S/L_S)(V_{GS} - V_{th})} \tag{4}$$

As M1 works in the triode region, the voltage between the node X and the node S is small, so the following approximation can be made

$$V_{GX} - V_{th} = V_{GS} - V_{th} - V_{XS} \approx V_{GS} - V_{th} \tag{5}$$

Bearing in mind that $W_D = mW_S$ and $L_D = L_S = L_{mín}$, the transconductance of M2 is

$$g_{m,D} \approx m r_{o,S}^{-1} \tag{6}$$

Figure 7 shows the small signal model for low and medium frequencies of the two series-connected transistors. The drain current through the transistors in series is

$$i_o = g_{m,D}(v_g - v_x) + \frac{v_o - v_x}{r_{o,D}} \tag{7}$$

$$i_o = \frac{v_x}{r_{o,S}} \tag{8}$$

From (7) and (8)

$$i_o = \frac{g_{m,D} r_{o,D}}{r_{o,S} + r_{o,D} + g_{m,D} r_{o,D} r_{o,S}} v_g + \frac{1}{r_{o,S} + r_{o,D} + g_{m,D} r_{o,D} r_{o,S}} v_o \tag{9}$$

According to this, the current i_o can be expressed as

$$i_o = g_{m,eq} v_g + \frac{v_o}{r_{o,eq}} \tag{10}$$

where

$$r_{o,eq} = r_{o,S} + r_{o,D} + g_{m,D} r_{o,D} r_{o,S} \tag{11}$$

$$g_{m,eq} = \frac{g_{m,D} r_{o,D}}{r_{o,S} + r_{o,D} + g_{m,D} r_{o,D} r_{o,S}} \tag{12}$$

Simplifying these expressions

$$r_{o,eq} \approx (m+1) r_{o,D} \tag{13}$$

$$g_{m,eq} \approx g_{m,D}/(m+1) \tag{14}$$

From (10) the small signal model of the equivalent transistor is the one in Fig. 8 where $r_{o,eq}$ is the output resistance and $g_{m,eq}$ the transconductance of the composite device. These expressions coincide with the output resistance and transconductance of a transistor whose width is the same as that of M_D and whose channel is $m+1$ times longer.

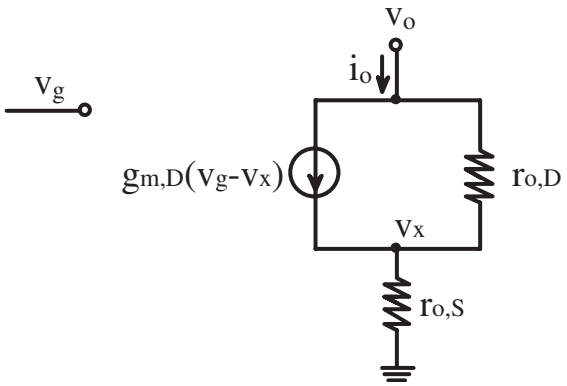

Fig. 7 *Small signal modelling of the self-cascode transistor (two transistors in series)*

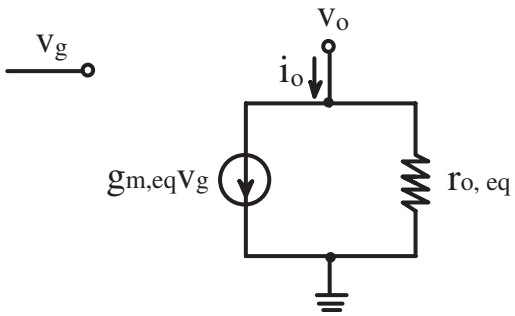

Fig. 8 *Small signal modelling of the self-cascode transistor (equivalent device)*