Analog Integr Circ Sig Process (2006) 48:263–266
DOI 10.1007/s10470-006-8245-z

MIXED SIGNAL LETTER

Low-voltage low-power 100 MHz programmable gain amplifier in 0.35 μm CMOS

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Received: 7 December 2005 / Revised: 9 March 2006 / Accepted: 10 March 2006 / Published online: 15 May 2006

Abstract This paper presents a low-voltage low-power intermediate-frequency programmable gain amplifier (PGA). To achieve low-voltage low-power and wideband operation while preserving linearity, the proposed cell is based on a very simple g_m-boosted differential pair degenerated with a hybrid polysilicon-MOS programmable resistor structure. Fabricated in a 0.35 μm CMOS technology, the PGA consumes less than 0.5 mW at a single 1.8 V supply. Measured results for a 3-bit implementation show a 0 to 18 dB linear-in-dB programmable gain with a constant bandwidth of 100 MHz when driving 150 fF capacitive loads. Distortion levels are below -72 dB over the whole gain range at 10 MHz for a 0.2 V_{p-p} differential output. Compared with other previously reported designs, it shows a good trade-off when all PGA parameters are considered.

Keywords CMOS analogue integrated circuits · Continuous-time systems · Low-voltage low-power design · Programmable gain amplifier

Introduction

Programmable gain amplifiers (PGAs) are essential blocks in many high frequency mixed-signal IC applications, such as wireless communication systems [1] and hard-disk-drive channels [2]. They typically work in a feedback loop that performs digital automatic gain control (AGC) in order to optimize the dynamic range of the succeeding circuits. To obtain the best overall performance, the PGA should neither limit the frequency operation nor the linearity of the system. In addition, the market has pushed the industry to the implementation of monolithic CMOS circuits to improve reliability and trim time-to-market. Therefore, low voltage circuit design techniques are mandatory. Furthermore, low power and area consumption architectures are also becoming necessary, especially in the portable equipment market. In CMOS technology, designing a low voltage PGA with wide bandwidth, high linearity and acceptable power consumption is a challenge and the purpose of this work.

This paper describes a fully differential programmable gain amplifier supplied at a single voltage of 1.8 V in a standard 3.3 V - 0.35 μm CMOS technology. To achieve a good trade-off between power dissipation, linearity, bandwidth and area consumption it is based on a very simple widely tunable differential pair degenerated with a combined MOS-polysilicon resistor network. Both the circuit principle and the degeneration scheme are first discussed. Next, the main PGA performances are summarized and finally conclusions are presented.

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Amplifier architecture

The proposed PGA, shown in Fig. 1, is based on a very simple g_m-boosted source degenerated differential pair with resistive loads. Focusing on the transconductor core, transistors M_1-M_2 form a two-pole negative-feedback loop that reduces the equivalent source resistance of the input

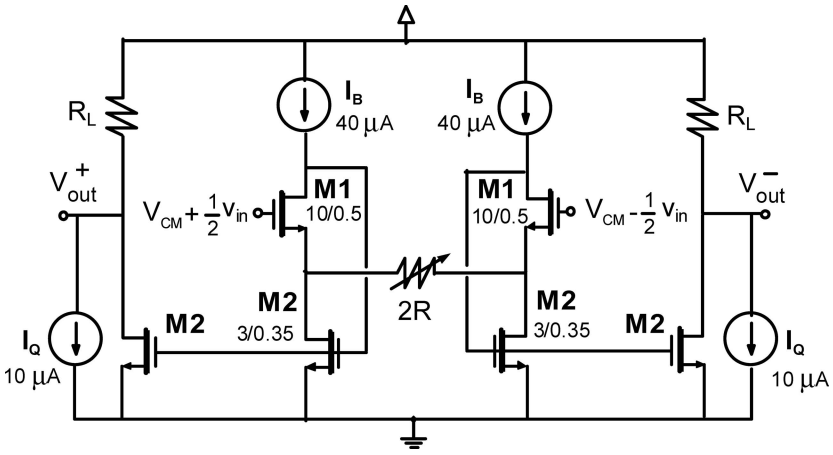

Fig. 1 Scheme of the proposed PGA

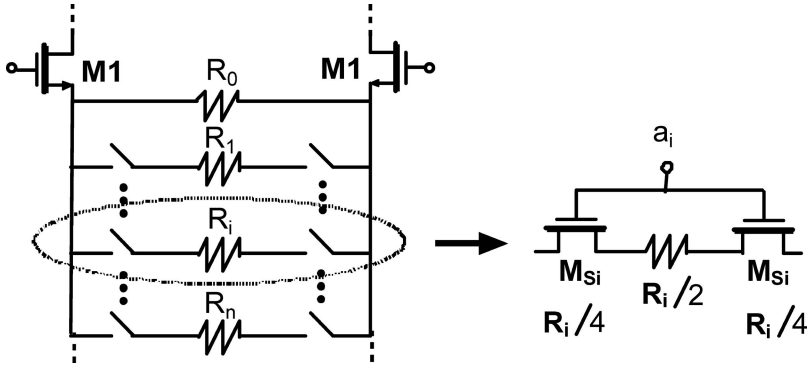

Fig. 2 Programmable degeneration resistor network

voltage buffer M_1 down to 50 Ω, value approximately given by $1/[g_{m1}g_{m2}(r_{01}//r_B)]$[1] where all parameters have their usual meaning and r_B is the Norton resistance of the current source I_B [3, 4]. Consequently, for a source-degenerated pair exploiting this approach, the differential transconductance can be expressed as α/R, where α denotes the M_1 gate-to-source DC voltage gain, which is somewhat less than unity due to the body effect, and R denotes one-half the degeneration resistance. The simplicity of this modified differential pair makes it very attractive for high-frequency and low-voltage low-power operation, conditions we are interested in.

Next, the linearized differential signal current, copied out by loading each M_2 gate terminal with a matched NMOS device, is converted to voltage through load resistors R_L. Thereby, the differential gain of this stage is given by $\alpha\cdot\ (R_L/R)$. The gain can be adjusted by using a variable degeneration resistor while maintaining a constant load resistor. This choice, adopted in this work, results in a fixed dominant pole at the PGA output nodes and therefore a constant bandwidth is maintained throughout all the gain stages [5]. For high-frequency applications, noise specifications limit the value of the load and degeneration resistors to the kΩ range. Hence, a high-resistive polysilicon (HRP) load resistor $R_L = 10$ kΩ has been chosen. With respect to the degeneration resistance, to preserve good linearity, moderate area consumption and, at the same time, facilitate digital gain control, we settled for an approach which combines, in equal parts, HRP resistors and MOS transistors biased in the triode region. These act simultaneously both as resistors and switches.

Following this strategy, the proposed degeneration scheme is shown in Fig. 2. The minimum gain setting is imposed by a fixed resistor R_o. The gain is then digitally controlled by adding in parallel a new linear resistor in series with two M_S NMOS switches, whose on-resistance is one half of the total impedance. Fine gain tuning can, if necessary, be performed through slight M_S gate voltage variations to improve accuracy. Finally, to guarantee a convenient common-mode output signal, controllable biasing currents I_Q are added to the two output nodes.

PGA implementation and performances

A PGA has been implemented in a 0.35 μm standard CMOS process employing the aforementioned structures as building blocks. Transistor sizes and values of current

[1] This source impedance contains a high frequency inductive component; however this inductive effect has negligible influence within the PGA frequency range of operation and will thus be neglected.

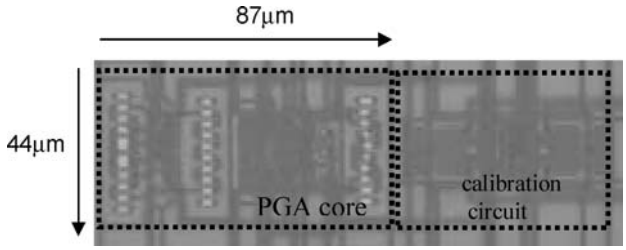

Fig. 3 PGA photograph

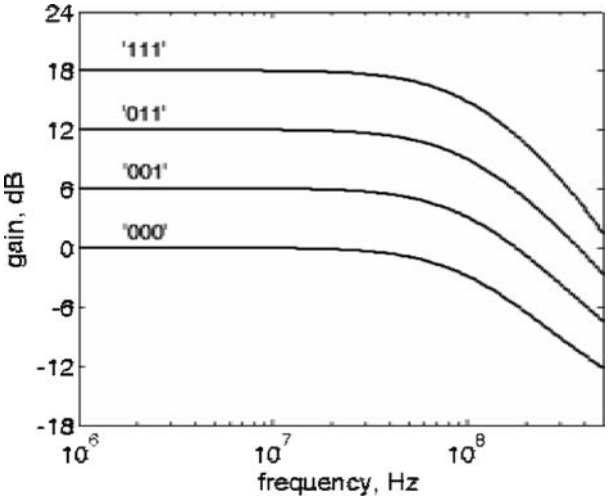

Fig. 4 PGA gain responses

are given in Fig. 1 and the photograph is shown in Fig. 3. It includes a calibration circuit for the measurement of the gain characteristic at high frequency in spite of the *I/O* parasitic elements. The cell, supplied at a single voltage of 1.8 V with a common-mode voltage of 1.3 V, dissipates less than 0.5 mW. The programmable degeneration impedance consists of a 3-bit array of hybrid NMOS-HRP resistors in parallel, which are weighted to obtain a logarithmic gain distribution ranging from 0 to 18 dB in 6 dB steps through a thermometer code control, as shown in Fig. 4. The experimental bandwidth is kept constant around 100 MHz assuming capacitive loads of 150 fF at the two differential outputs. The measured total harmonic distortion (THD) levels at 10 MHz are below −72 dB over the whole range for a differential output signal of 0.2 V_{p-p}, value that increases

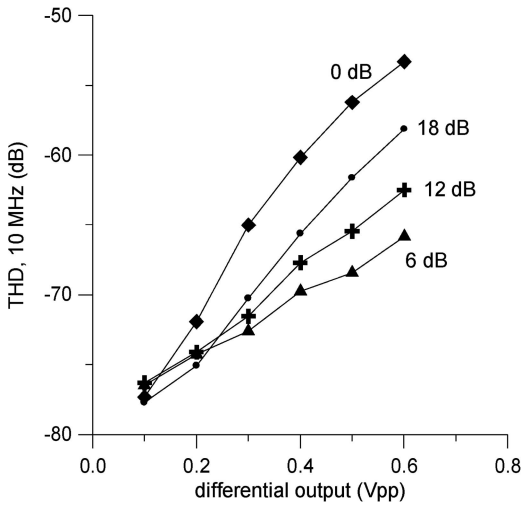

Fig. 5 THD levels at 10 MHz for all gain settings

to −60 dB for 0.4 V_{p-p} (Fig. 5). Measurements for an input signal frequency of 30 MHz maintain these reported THD limits. The simulated in-band noise at 0 dB is 51 nV/$\sqrt{}$Hz.

The main performances of the proposed design are compared in Table 1 with those of several previous realizations: references [5–7], all using switched banks of linear resistors to obtain a comparable gain range. The proposed circuit has a bandwidth just as large as other published PGAs for similar technologies, but at a lower supply voltage of 1.8 V and with a significantly lower power consumption and area. On the other hand, with our design, as well as with [5], linearity is limited by the open loop nature of the amplifier. The configurations described in [6, 7] use amplifiers operating in closed loop with a resistive feedback network, thus obtaining better distortion levels at a cost of higher power consumption.

Conclusions

A low-voltage 3-bit programmable gain amplifier has been successfully implemented in a 0.35 μm CMOS process showing a good trade off between power consumption, maximum operating frequency and linearity. Further scaling of the gain step resolution is possible to employ this

Table 1 Comparison of several PGA performances

Design	[5]	[6]	[7]	This work
CMOS process (μm)	0.5	0.35	0.25	0.35
Supply voltage (V)	5	3.3	2.5	1.8
Power (mW)	25	21	6.75	0.42
Intrinsic BW (MHz)	60*	125	100	100
Gain range (dB)	−2 to 12	0 to 19	5.6 to 17	0 to 18
Linearity at 10 MHz				
V_{pp-out}/V_{supply}	0.2	0.6	0.56	0.22
THD (dB)	−60	−74	−67	−60
Active area (mm^2)	0.175	0.18	0.038	0.004

*Estimated BW. Measured BW = 15 MHz, limited by the test probe.

digitally programmable gain section as a building block for the AGC circuit in IF strips. Furthermore, the design can be easily migrated to a 0.18 μm 1.8-V CMOS process.

Acknowledgment This work has been partially supported by DGA-FSE (PIP/187-2005) and MCYT-FEDER (TIC2005-00285/MIC)

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