Low-Cost TIA and Equalizer for SI-POF

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Abstract: This paper presents an analog front-end suitable for low-cost POF systems compatible with the standard IEEE 1394b. The proposed front-end includes a Si PIN photodiode, a transimpedance amplifier and a differential equalizer.

1. Introduction

A great interest has emerged in the use of plastic optical fibers (POFs) for data transmission systems. The low cost of manufacture and maintenance of such systems makes them very attractive for the consumers. For this reason, recently the standard IEEE 1394b includes the requirements of a POF system in local area networks [1].

The analog receiver front-end appears as one of the most important blocks because it sets the network performance. Given this consideration, in the last years several alternatives of analog front-ends have been reported, [2-4]. In all these proposed designs the conventional architecture includes a low cost silicon photodiode (PD), a transimpedance amplifier (TIA) and a continuous-time equalizer (EQ).

Precisely in this work, a complete analog front-end is presented. In section 2, the design of the front-end is introduced. In section 3, the results will be shown, and at the end, the main conclusions will be drawn.

2. Design of the front-end

2.1 Fiber and photodiode

In order to implement a suitable analog front-end, the designer needs to know the signal transmission and detection characteristics of the fiber and the photodiode, respectively.

Taking into account the strong dependence of the fiber bandwidth on the length, the first step was to measure the bandwidth of the POF (ESKA Premier GH 4002 2.2 mm) with lengths of 10, 20 and 30 m. It was tested following the approach reported in [5]. The results are shown in Fig. 1.

The choice of the photodiode represents the second critical design criterion. Nevertheless, if the aim is a low cost system, silicon photodiodes is the best option. In our case, a S5972 Si PIN Photodiode (Hammamatsu) has been selected.

To get a good characterization of the photodiode, an analysis was made of its depletion capacitance, C_{PD}, versus the reverse bias voltage, V_{REV}. This analysis is shown in Fig. 2. These results show that for $V_{REV} \geq 1.5$ V, the value of C_{PD} remains almost unchanged in 3 pF.

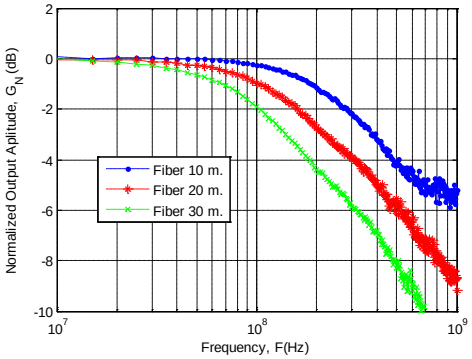

Fig.1. Frequency response of the POF GH 4002 with different lengths.

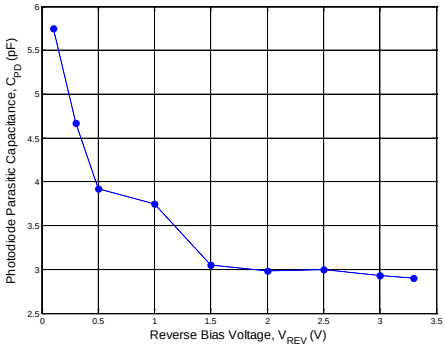

Fig. 2. Photodiode capacitance as a function of the reverse voltage.

2.2 Transimpedance amplifier

In this work, a shunt-feedback TIA designed with a passively loaded bipolar transistor is proposed. The structure is depicted in Fig. 3.

As shown in this figure, an input matching network is also included. This is based on a bias resistor, $R_{PD} = 2$ kΩ, and a decoupling capacitor, $C_D = 22$ nF. The resistor value is calculated for reduced impact in the frequency response and the capacitor avoids the pernicious DC offset input current. One important design condition is $R_{PD} >> Z_{in}$ where Z_{in} represents the input impedance and whose value is around 100 Ω.

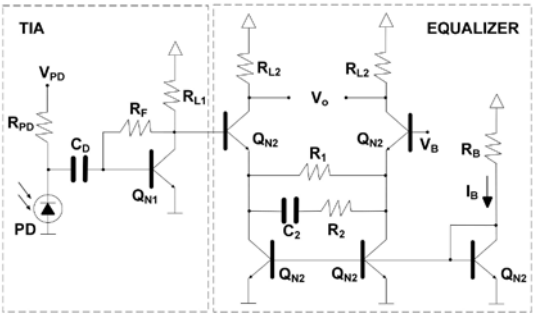

Fig. 3. Schematic of the proposed front-end.

The transistor Q_{N1} is the key device in this input block. The transresistance, the bandwidth and the noise, fundamental specs in a TIA, depend strongly on it. The optimization of this transistor is done in two different ways: First, choosing proper commercial devices and then maximizing the channel capability in the Shannon sense.

In this work, a BFP640 NPN Silicon Germanium RF Transistor, with packaging SOT343 (Infineon), is selected for the implementation of Q_{N1}. This transistor has a transition frequency of 40 GHz. This transition frequency guarantees as main frequency limitation the photodiode depletion capacitance, which has been well characterized in the previous section.

Shannon´s equation in [6] allows obtaining the expression of the TIA capability, C, given by:

$$C = BW \cdot \log_2 \left(\frac{i_{in} + \left(\bar{i}^{\,2}_{n,TIA} \right)^{\frac{1}{2}}}{\left(\bar{i}^{\,2}_{n,TIA} \right)^{\frac{1}{2}}} \right) \tag{1}$$

where BW, i_{in} and $i_{n,TIA}$ represent the bandwidth, the input signal amplitude and the input-referred noise, respectively. Applying small-signal models for each device of the TIA, analytical are obtained:

$$T_R \approx (\beta \cdot R_{L1}) \| R_F \tag{2}$$

$$BW \approx \frac{1}{2\pi \cdot \left(\frac{C_{in}}{\beta} + C_{bc} \right) \cdot T_R} \tag{3}$$

$$\bar{i}^{\,2}_{n,TIA} \approx \left(\frac{4kT}{R_F} + \frac{2qI_C}{\beta} \right) BW_n \tag{4}$$

In these equations T_R represents de transresistance of the TIA, β is the current gain of the bipolar transistor Q_{N1}, C_{in} is the input parasitic capacitance of the TIA and C_{bc} is the base-collector capacitance. C_{in} includes the PD depletion capacitance, C_{PD}, the base-emitter capacitance, C_{be}, and the parasitic capacitance of the track, C_{TRACK}. Similarly, I_C is the collector current and $BW_n = 1.1 \cdot BW$ is the effective white noise bandwidth. The rest of the magnitudes have the conventional meaning, [7-8].

All the previous intrinsic magnitudes have dependence on the bias current. These dependences are quite complicated in some cases, and for this reason the value of each magnitude is directly extracted from the simulator. Keeping in mind this fact, the theoretical results of the normalized capability of the proposed TIA are those shown in Fig. 4.

In these results, the biasing was defined in each point for optimum output dynamic range and for optimum bias point of the next stage (the equalizer). For this reason, given a specific bias current, resistors R_F and R_{L1} in Fig. 3 were calculated to set V_{CE} to 1.75 V. Similarly, another factor which must be taken into account is that the input current is around 1 μA.

Although the optimum capability is obtained within I_C = 40 mA, our definitive choice was I_C = 30 mA, R_F = 4 kΩ and R_{L1} = 50 Ω. These values are chosen for two reasons: 1) the proper output matching impedance is obtained and 2) the C improvement between the two previous currents does not justify the increase in the power consumption. Final calculated specs are: $T_R \approx 70$ dBΩ, BW≈ 251 MHz and $i_{n,TIA} \approx 125$ nA_{rms}.

2.3 Equalizer

The proposed equalizer is shown in Fig. 3. It is based on a bipolar degenerated pair with a RC compensation network. All bipolar transistors are implemented by using a commercial HFA3127 NPN bipolar array with package SOIC (Intersil). In this way, a good tracking between paired transistors is obtained achieving a better differential response. The transition frequency is 8 GHz.

The optimization of the equalizer capability mainly implies the optimization of the frequency response. However, given the signal levels required by the limiting amplifier (next block in the receiver), certain gain factors must be guaranteed. The simulated results of the equalizer capability as a function of the bias current are shown in Fig. 5.

Again, the biasing was defined in each point to obtain the optimum output dynamic range. For this reason, given a specific bias current, the optimum R_{L2} was calculated to set the DC output level to 1.75 V.

Although the optimum capability is obtained within I_C = 50 mA, to reduce the power consumption and to get an output matching impedance (R_{L2} = 50 Ω) I_C = 30 mA was chosen. These values provide a gain G ≈ 17 dB and a minimum BW ≈ 600 MHz (without equalization network).

Once the pair is optimized, the RC compensation network must be designed. Equation (5) presents the equalizer transfer function where the dependence on the intrinsic parameters is shown. The parameter r_{be} represents the base-emitter resistance. The transfer function has in first order approximation a zero and a pole.

$$H(s) \approx \frac{\beta R_L}{r_{be}+(\beta+1)R_1} \cdot \frac{1+sC_1(R_1+R_2)}{1+s\dfrac{C_1(r_{be}(R_1+R_2)+(\beta+1)R_1R_2)}{r_{be}+(\beta+1)R_1}} \tag{5}$$

In order to get a well designed equalizer an iterative process based on comparison between theoretical and experimental results is employed. In this work, the network is changed manually by simple manipulation of the PCB. In the definitive version the change of the compensation network will be done electronically by means of an ADG904 digital RF switch array (Analog Devices). The final network values will be shown in the next section.

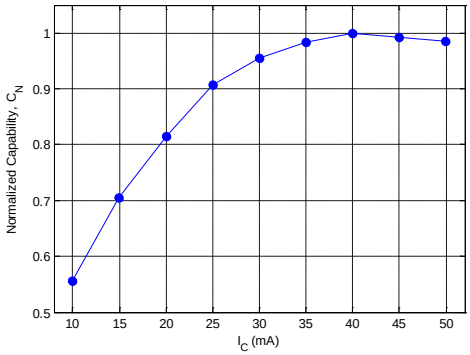

Fig. 4. Normalized TIA capability as a function of the bias current.

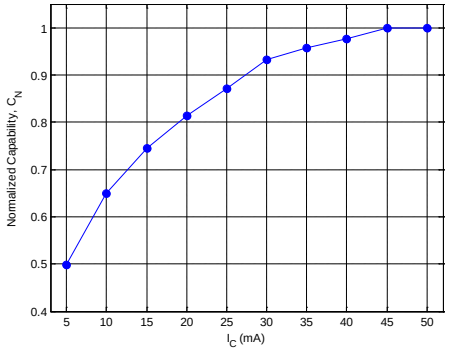

Fig. 5. Normalized equalizer capability as a function of the bias current.

3. Experimental results

The proposed design was mounted in a double-sided PCB, see Fig. 6. One of these sides is a uniform ground plane where the PD is soldered (bottom). The other is used for signal and supply routing (top). The whole system power consumption is 396 mW with a single 3.3 V supply voltage.

Our test circuit includes another PCB where a DL3149-057 red laser diode (Sanyo) with a 50Ω matching network is employed. This test laser is routed by using a bias-T ZFBT-4R2G+ (Minicircuits).

The results in Fig. 7 correspond to the frequency response of the whole circuit measured with a ZVL 6 GHz network analyzer (R&S). This analysis considers different fiber lengths with the adequate compensation network. These results are compared with those obtained when no equalization is made. This comparison shows a bandwidth enlargement between 3.7 and 4.6 times, depending on the fiber. It is quite interesting to note that the output cut-off frequency is almost constant despite of the variable input cut-off frequency. This confirms the proper system operation.

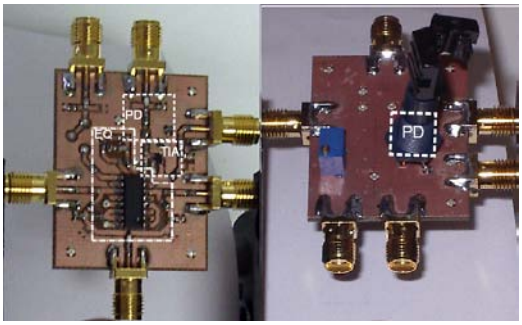

Fig. 6. Whole proposed analog front-end.

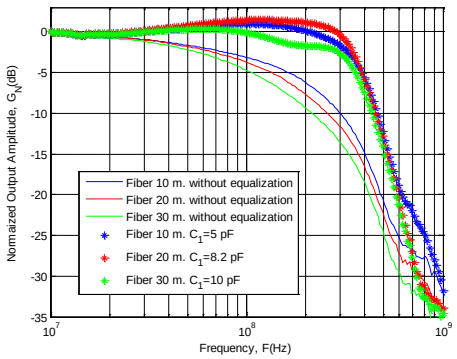

Fig. 7. Frequency response of the analog front-end.

Fig. 8, 9 and 10 show the experimental eye diagrams of the whole circuit measured with an Infiniium DCA-J 86100C digital communications analyzer (Agilent) and a N4906A bit error rate tester (Agilent). All results consider a 2^{31}-1 non-return to zero pseudorandom bit sequence (NRZ PRBS) at 800 Mb/s and the same transmitted optical

power. Eye diagrams show a variation in the eye opening from 3 mV to 24 mV, obtaining the smallest result with the fiber of 30 m. Nevertheless, all cases achieve a BER lower than 10^{-12}. The worst jitter is 170 ps_{rms} for the fiber of 30 m.

Fig. 11 presents the output noise distribution as a function of the 1/0 logical state. The maximum experimental noise contribution is detected when the state is 1 achieving 614 μV_{rms} while our theoretical models predict 410 μV_{rms}.

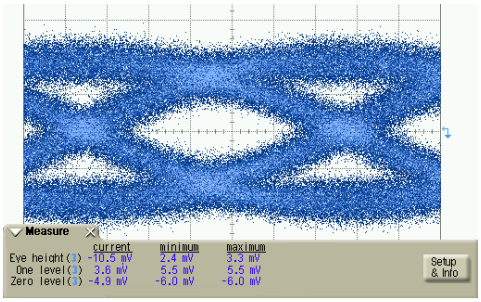

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5 Ω, C_2 = 10 pF, 30 m fiber length and 800 Mb/s.

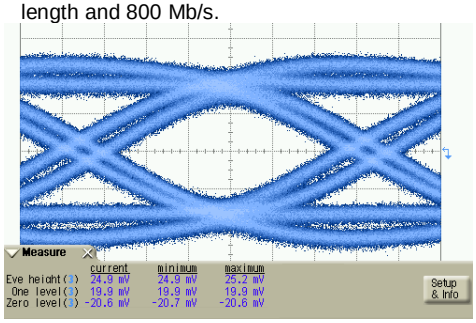

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5 Ω, C_2 = 5 pF, 10 m fiber length and 800 Mb/s.

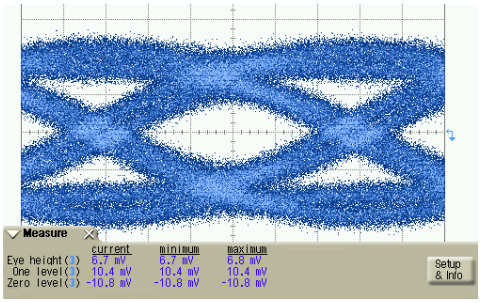

Fig. 10. Eye diagram at 2^{31}-1 NRZ PRBS. R_1=220 Ω, R_2 = 5 Ω, C_2 = 8.2 pF, 30 m fiber length and 800 Mb/s.

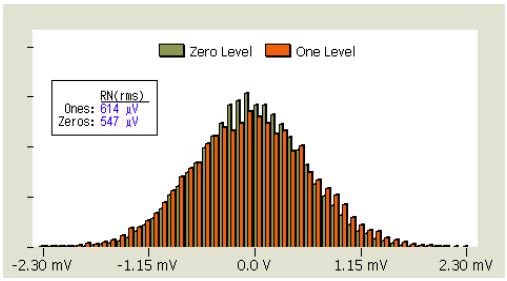

Fig. 11. Output rms noise distributions.

4. Conclusions

This paper has presented an analog front-end suitable for low-cost POF systems in the standard IEEE 1394. The proposed front-end includes a Si PIN photodiode, a transimpedance amplifier and a differential equalizer. The analog front-end has been designed in bipolar technology with supply voltage of 3.3 V. The whole system consumes 396 mW, achieves a total gain of 70 dBΩ and operates up to 800 Mb/s. At this bit rate and with fiber lengths up to 30 m, the circuit has a BER $\leq 10^{12}$ and a maximum jitter of 170 ps_{rms}.

Acknowledgements

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