

Low-cost, digital lock-in module with external reference for coating glass transmission/reflection spectrophotometer

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Received 8 October 2002, in final form and accepted for publication
27 February 2003

Published

Online at stacks.iop.org/MST/14/1

Abstract

A versatile, low-cost, digital signal processor (DSP) based lock-in module with external reference is described. This module is used to implement an industrial spectrophotometer for measuring spectral transmission and reflection of automotive and architectonic coating glasses over the ultraviolet, visible and near-infrared wavelength range. The light beams are modulated with an optical chopper. A digital phase-locked loop (DPLL) is used to lock the lock-in to the chop frequency. The lock-in rejects the ambient radiation and permits the spectrophotometer to work in the presence of ambient light.

The algorithm that implements the dual lock-in and the DPLL in the DSP56002 evaluation module from Motorola is described. The use of a DSP allows implementation of the lock-in and DPLL by software, which gives flexibility and programmability to the system. Lock-in module cost, under 300 €, is an important parameter taking into account that two modules are used in the system. Besides, the algorithms implemented in this DSP can be directly implemented in the latest DSP generations.

The DPLL performance and the spectrophotometer are characterized. Capture and lock DPLL ranges have been measured and checked to be greater than the chop frequency drifts. The lock-in measured frequency response shows that the lock-in performs as theoretically predicted.

Keywords: lock-in, coating glass, transmittance measurement, reflectance measurement, spectrophotometer

Ascii/Word/MST/mst154401-xsl/PAP
Printed 12/3/2003
Issue no
Total pages
First page
Last page
File name E .TEX
Date req
Artnum
Cover date
(Ed: SARAH)

1. Introduction

Q.1 The aim of developing a lock-in card was to include two of them in an industrial spectrophotometer for measuring spectral transmission and reflection of automotive and architectonic coating glasses with energy control properties (low emissivity and solar control coatings [1]). An accurate and fast measurement of optical transmission and reflection properties over the ultraviolet, visible and near-infrared (UV-vis-NIR) wavelength range (300–2500 nm) allows us to characterize the solar and luminosity factor of a coating glass sample in order to control the production process of multilayers in real

time. This system should measure in an industrial environment with ambient light and electrical noise, that is why a lock-in (or phase sensitive) technique is used in the light detection system.

Initially, lock-ins were implemented with analogue techniques. However, during the past 35 years, it has been increasingly recognized that digital techniques could improve certain aspects of the lock-in performance. Advantages of the digital lock-in have been claimed in the literature [2–14], such as the extension of the carrier frequency range to arbitrarily low values, extension of the filter time constants to both shorter and longer values, the rejection of unwanted DC and low-frequency signals and reduced drift, among others.

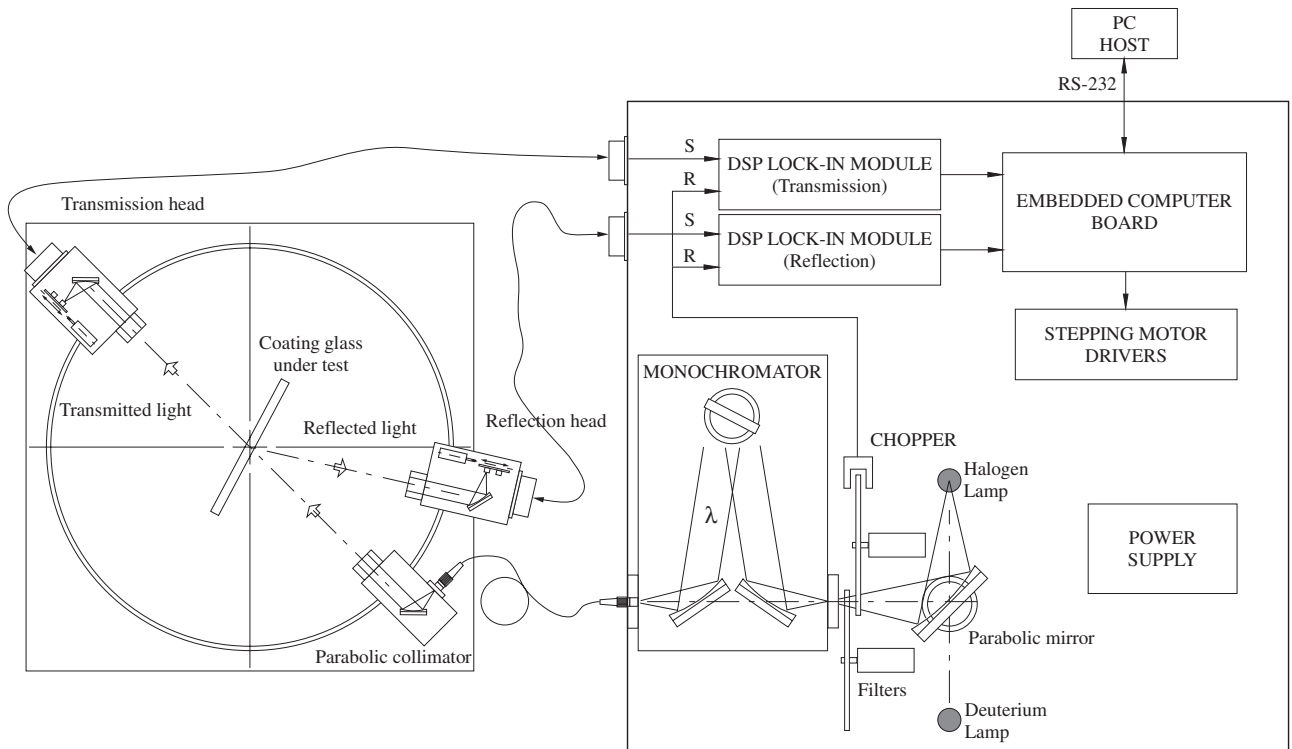


Figure 1. Schematic of spectrophotometer.

Digital lock-ins are not a recent development; they appeared over 30 years ago [2]. The published literature on digital lock-ins falls into two categories: first, the hardware-based digital lock-ins that require the construction of specific electronics [5–8]; second, the software-based versions that are constructed with commercially available boards or instruments connected or not to a personal computer [9–15]. Of course, there are also commercially available digital lock-ins [16].

This paper proposes a versatile, low-cost and modular digital lock-in with external reference based on a digital signal processor (DSP) evaluation board. The use of digital processing techniques in a DSP allows us to implement the lock-in algorithm by software. That allows flexibility, programmability, easy development and debugging. Moreover, this implementation is modular, making it easy to house the lock-in module in the system crate.

A DSP-based lock-in that operates with a reference frequency generated internally is described in [15]. But, this lock-in cannot be used in the spectrophotometer because the light sources are lamps that cannot be modulated electrically. The light signals must be modulated externally with optical choppers. In this case, a phase-locked loop (PLL) must be included to lock the lock-in to the chop frequency. This is one of the innovations that have been developed in this work with regard to [15].

First, this paper outlines the block diagram of the spectrophotometer system that can measure spectral transmission and reflection of coating glass simultaneously. Section 3 describes the fundamentals of the lock-in theory. Sections 4 and 5 present some considerations about hardware and software implementation of different parts of the algorithm, with special attention to the digital phase-locked loop (DPLL). Finally, based on experimental tests, DPLL, lock-in and spectrophotometer performance is characterized.

2. Spectrophotometer system

The requirements for the spectrophotometer system were the following ones. First, the system should measure in an industrial environment with ambient light and electrical noise, then precautions are needed in order to make a reliable system, particularly in the light detection system. Second, the system should measure quickly, and then simultaneous measurement of reflection and transmission is required. Also, communication with an external PC host is necessary to control the whole system.

A schematic diagram of the developed spectrophotometer is shown in figure 1. The system contains two light sources. A 20 W deuterium lamp is used for the UV spectral range. A 35 W halogen lamp is used for the vis–NIR wavelength range. A collection parabolic mirror focuses the radiation on the monochromator entrance slit and it can be rotated to select either of the two lamps. At the monochromator input, an optical chopper modulates the light and generates the lock-in reference input, and a motorized set of filters avoids harmonics of the grating. The monochromator (CVI CM110) selects the wavelength radiation. It has two gratings (UV–vis and IR) with 1200 and 600 lines mm^{-1} respectively. Light at the monochromator output is guided by a fibre optic to an off-axis parabolic collimator. The collimator and the detectors are housed in three holders or heads mounted on a rotation stage (see figure 1). It allows us to rotate the holders at a constant radius around the glass sample. At the selected incident angle, one of the holders detects the beam transmitted through the glass sample and the other the reflected beam.

Each detector holder has two sensors; an Si photodiode is used for the UV–vis spectral range and an SPb resistor for the NIR regions. A stepping motor shifts the sensors,

and controls in which of them the light is focalized. A low-noise transimpedance amplifier is used with the Si photodiode detector and a voltage amplifier with the SPb resistor.

Two low-cost lock-in amplifiers, as described in this paper, locked to the chop frequency, process transmission and reflection signals. The results are transferred to the embedded computer board WAFER-4823 from ICP-Electronics. This board contains a DX4-100 CPU and it is connected to a PCM-3730 digital I/O module from Advantech. The embedded computer board through the I/O module generates signals to control the motion and limits of the stepping motors, handles data acquisition from the lock-in modules and configures the filter cut-off frequency. There are four stepping motors: one motor to select the lamp source, another one to select the second-harmonic cut-off filter at the monochromator input and two to move the detectors in transmission and reflection heads. The embedded computer has two RS-232 serial ports. One serial port is used to control the monochromator and other to communicate with an external PC host. The PC host acts as the master and the embedded computer as a slave. The PC sends to the embedded computer several parameters: computer spectrophotometer setting conditions, wavelength selection, switch on/off of sources and integration time of lock-in cards. The embedded computer transfers to the PC the lock-in measurements for plotting and analysis.

The PC host runs the visual interface software, which was developed using Microsoft Visual Basic for Excel under WindowsTM 98. This high-level language provides both the tools for controlling the slave embedded computer via the RS-232 serial port and an easy way to show and arrange the final results with the use of tables and graphics. Meanwhile, the single-board slave computer executes, under MS-DOS, a C-coded program with two basic functions: the interpretation and—if necessary—redirection of the orders received from the master computer, and the generation, through the digital I/O module, of the series of pulses needed to control the stepping motors. Thus, real-time tasks are run on the DSP and system-level tasks are implemented on the PC host.

From now on, we concentrate on the lock-in card description, with special emphasis on the DPLL that locks the chop frequency.

3. Lock-in amplifier with external reference

Lock-in measurements require a frequency reference f_r . Typically, an experiment is excited at a fixed frequency f_r and the lock-in detects the response from the experiment at the reference frequency f_r . The response of a phase sensitive detector depends on the phase difference between the signal and the reference. This phase dependence is eliminated by adding a second phase sensitive detector, that is why a dual-phase lock-in is used.

A block diagram of a dual-phase lock-in with external reference R is shown in figure 2. Let the input signal S be a sine wave of frequency f_r :

$$S = V_S \sin(2\pi f_r t + \theta_S).$$

The reference signal R is the square wave generated by the optical chopper of the spectrophotometer described in figure 1

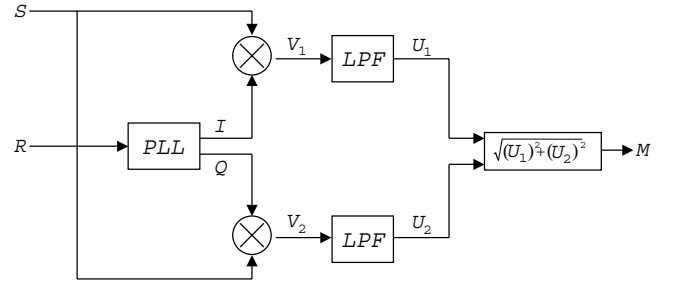


Figure 2. Dual-phase lock-in block diagram.

and f_r is the chop frequency. A PLL locked to the external reference R generates two internal reference sine signals I and Q of frequency f_L in quadrature,

$$I = V_L \sin(2\pi f_L t + \theta_L) \quad Q = V_L \sin(2\pi f_L t + \theta_L + \pi/2).$$

Then, signal S is combined with the two locally derived reference signals. The PLL makes the reference signal frequency f_L equal to the signal frequency f_r and keep the phase between them constant in time. Then, a dc output M proportional to the amplitude of the input signal S is obtained from the in-phase and quadrature components,

$$M = \sqrt{U_1^2 + U_2^2} = \frac{V_S V_L}{2}.$$

If the input signal S is multiplied directly by the square wave signal R , the lock-in will be sensitive to all Fourier components of R (a square wave contains many large odd harmonics). That is why a PLL is used to generate two high-purity sine waves in quadrature, phase locked with the driven signal R . Besides, in order to work properly, the reference signals must be phase locked to the reference. Since PLL actively tracks the external reference R , changes in R frequency do not affect the measurement. The resulting system is said to have ‘fundamental-only’ response [3].

Lock-in behaves like a band-pass filter centred on the reference frequency f_r , with a bandwidth equal to twice the bandwidth of the LPF, removing the noise at other frequencies. Thus, it is applicable to the classic signal to noise improvement factor for the recovery of signals from white noise by filtering [4]:

$$\frac{SNR_O}{SNR_I} = \frac{BW_I}{BW_O}$$

where BW_I is the input noise bandwidth and BW_O is the filter bandwidth. The value of f_r must not coincide with any harmonic of the mains frequency in order to reduce interference.

The basic PLL consists of a phase detector (PD), a low-pass filter (LPF) and a voltage-controlled oscillator (VCO). The VCO attempts to produce a signal that is synchronized with the PLL input in frequency as well as in phase. The PD measures the phase error between the PLL input and the VCO output. The resulting error is filtered to suppress the noise and high-frequency signal components from the PD and provide a dc control signal for the VCO. The implemented PLL is described in section 5.

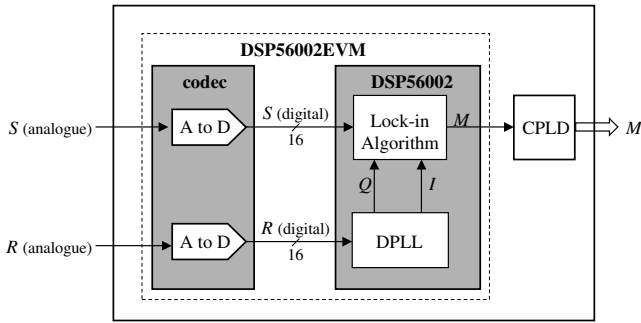


Figure 3. Functional schematic diagram of the lock-in card.

The frequency range over which the PLL output frequency will move to the reference frequency is called the capture range of the PLL, and the frequency range over which the PLL will maintain lock but over which it will not necessarily acquire lock is called the lock range of the PLL [21]. The lock range is greater than or equal to the capture range.

4. Hardware and software architecture

The dual-phase lock-in has been implemented on the DSP56002EVM evaluation module from Motorola. In [15, 17], this or similar DSP modules are used to implement measurement or signal processing systems respectively. This evaluation module contains a 24-bit DSP56002 DSP [18], the CS4215 audio codec, external static RAM for expansion memory and EEPROM for stand-alone operation. The CS4215 is a single chip with two channels of 16-bit analogue-to-digital conversion (ADC) and two channels of 16-bit digital-to-analogue conversion (DAC).

We have used this evaluation module because it is a low-cost, fully assembled and tested printed circuit containing a DSP and stereo ADC and DAC which makes it ideal for implementing low-frequency processing algorithms. Besides, it allows stand-alone operation using an EEPROM to store the program, and a great variety of assembler programs for this DSP are available free of charge from the Motorola DSP web site.

A functional schematic diagram of the lock-in card is shown in figure 3. The signal to measure S and the reference signal R are connected to the stereo line in input in the DSP56002EVM. These inputs are AC coupled to the codec ADCs with a programmable gain block. Then, the codec passes the 16-bit digitized signals S and R to the DSP chip. According to CS4215 codec specifications, the interchannel isolation has a typical value of 80 dB. Thus, a fraction of the reference signal will be added to or subtracted from the actual signal and cause errors in the measurement. Moreover, the lock-in cannot reject this coupled ‘noise’ because the added noise is at the reference frequency. To minimize the coupling, the square wave R is attenuated before being digitised; after that, the DSP compares the digitized signal R with zero, and converts it to a full numeric range square-wave signal that becomes an input signal to the PD.

The sample frequency is programmable from 4 to 48 kHz. The used sampling rate is limited by two factors: the maximum codec throughput rate, and the computational time required by the algorithm to be implemented. In this application, the

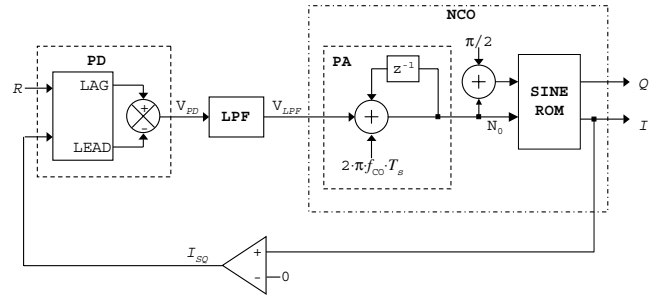


Figure 4. DPLL block diagram.

sampling rate of the codec has been programmed to be 8 kHz. The signal is filtered by the codec with an antialiasing on-chip filter that adapts to the sample frequency selected.

The references I and Q are multiplied by the signal S in the DSP chip. The filters implemented are IIR. The defining relationship between input and output variables for a n -order IIR filter is given by the difference equation

$$y(n) = \frac{1}{a_0} \left(\sum_{k=0}^N b_k \cdot x(n-k) - \sum_{m=1}^N a_m \cdot y(n-m) \right),$$

where $x(n)$ is the input signal sample and $y(n)$ is the corresponding output. Coefficients depend on the filter type and order. A second-order Butterworth LPF has been used because of its maximally flat passband. The cut-off frequency of the filters can be programmed to be 5.3, 1.6, 0.53 or 0.16 Hz. The selection is a trade-off between the noise reduction and the time response.

The effects of finite word length in the filter performance were analysed with MATLAB. The simulations show that the DSP double precision mode has to be used to minimize quantization errors. The square root in figure 2 is computed using a successive approximation technique.

The algorithm has been programmed using the assembler language of the DSP. The DSP is never interrupted. Every certain programmable time, the DSP writes the 24-bit digitized result M into a complex programmable logic device (CPLD) that is mapped into the Y DSP data memory. The CPLD implements a buffer in which the DSP writes and the embedded computer reads through the I/O card.

Once we have outlined above how the lock-in algorithm has been implemented in the DSP, we will concentrate on PLL implementation.

5. PLL implementation

The PLL has been implemented via software on the DSP. A block diagram of the implemented DPLL is shown in figure 4. It contains a PD, an LFP and a numerically controlled oscillator (NCO). The NCO is the digital counterpart of the VCO. R is the square-wave reference signal, I and Q are the digital sampled sine wave outputs that are locked to R and I_{SQ} is a digital square-wave signal generated from I via software and then applied to the PD.

There are different types of digital PD [19–21]. The implemented digital PD is the lag–lead PD [21]. It is sensitive only to the relative timing of edges between both signals and is completely independent of the duty cycle of the input

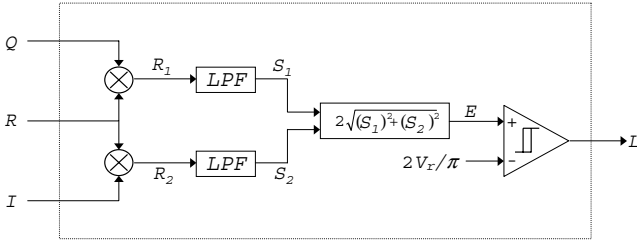


Figure 5. Locked state detector block diagram.

signals. It generates either lead or lag output pulses, depending on whether the transitions of I_{SQ} occur before or after the transitions of R , respectively. The PD output at the sample instant kT_S is

$$V_{PD}(k) = K_d(\text{lag} - \text{lead})$$

where T_S is the sampling period and *lag* and *lead* signals have numeric values of unity or zero. The resulting error signal V_{PD} is filtered to become the control signal V_{LPPF} that drives the NCO (see figure 4). The implemented LPF is a first-order 2 Hz low-pass Butterworth filter with unit gain. This LPF performs two functions: first, it provides a DC level proportional to phase error, and second, smoothes it by filtering. The NCO consists of a phase accumulator (PA) and a sine table. Since the PA adds angles (in radians), it must be a modulo- 2π adder. The output of the PA represents a phase and it can be written

$$N_0(k) = 2\pi f_{CO} kT_S + \phi(k)$$

where f_{CO} is the free-running frequency of the NCO and the phase $\phi(k)$ satisfies the difference equation

$$\phi(k) - \phi(k-1) = V_{LPPF}(k).$$

The sine table is a 256×24 -bit sine ROM that is mapped in the locations \$0100–\$01FF of DSP Y memory. This ROM contains all amplitude values for sine within $-\pi$ and π . The most significant byte of N_0 provides the address to the ROM. To increase resolution, the remaining bits of N_0 are used to perform a second-order (linear + quadrature) approximation between table points.

The DPLL lock range is the full NCO range and it can be expressed as $f_{CO} - (\Delta f_L/2) \leq f \leq f_{CO} + (\Delta f_L/2)$, where

$$\Delta f_L = \frac{K_d}{\pi T_S}.$$

Then, in order to increase the lock range, parameter K_d must be increased. However, with increased values of K_d , the frequency domain spectra of signals I and Q spread and the bandwidth noise is incremented as shown in the experimental section, then the performance of the lock-in as a band-pass filter deteriorates. Maintaining a narrow bandwidth is required for tracking input signals embedded in noise. Then, the K_d choice is a trade-off between lock range and bandwidth of the output signal of the DPLL. The DPLL lock range must be chosen to be greater than the chop frequency drift due to slow changes in the DC motor speed.

Lock-in measurements are not valid if the DPLL is not locked. To detect this situation, we have used the algorithm

based on the lock-in philosophy shown in figure 5. The binary output L is asserted if the DPLL has locked onto the reference signal R . Signal E has the value of the first harmonic of signal R ($2V_r/\pi$ assuming 0.5 duty cycle) when the system is locked. Signal E has a lower value in the other case. Then, the signal L is obtained by comparing E with the constant value $2V_r/\pi$. Hysteresis is applied to the comparison to avoid unwanted oscillations in L . This algorithm has been implemented in the DSP.

The whole DPLL system has been extensively simulated with MATLAB in order to get the optimum values for design parameters.

6. Experimental results

The experimental results described in this section relate, fundamentally, to analysis of DPLL, because experimental characterization of a lock-in system with internal synthesized reference was made in [15]. Amplitude and frequency measurements have been made with a $7\frac{1}{2}$ digit HP34401A multimeter and an HP33120A synthesizer as square wave reference signal source at 270.000 Hz, and the signal I of the DPLL output is routed to the line output of the DSP56002EVM board for analysis. Maximum, minimum and average amplitude and frequency are obtained using these specific functions of the HP34401A multimeter.

As we have seen in section 3, the magnitude M computed by the lock-in algorithm depends on V_L , the reference sine signal's amplitude. Maximum and minimum amplitude values of signal I in the DSP56002EVM line output have been measured for several values of K_d . The ratio of the fractional changes of signal I amplitude was found to be lower than 30 ppm for $K_d/\pi < 0.08$. Numerical stability must be even better because stereo D/A instabilities are included in the measurement. In any case, values are low enough to allow a correct working of the lock-in system.

With an input reference frequency signal of 270.000 Hz, the output averaged frequency of the signal I was measured for several values of K_d . The frequency error was found to be lower than 0.006 Hz for $K_d/\pi < 0.08$. This error is irrelevant for practical situations. In fact, the lower bandwidth LPF implemented in the lock-in algorithm has 0.16 Hz cut-off frequency and the system behaves as a band-pass filter of 0.32 Hz with central frequency displaced lightly to the frequency input of the DPLL ($\Delta f = 0.004$ Hz @ $K_d/\pi < 0.01$); however, this is still placed at the zone of maximum transmission of the filter.

We can compare, in table 1, the lock range of the DPLL, Δf_L , predicted theoretically and values measured experimentally for different values of K_d . A reference signal of 270.000 Hz is used and a central frequency of VCO, f_{CO} , of 270.000 Hz is programmed. We see a reasonable agreement between experimental and theoretical predictions.

In figure 6 we represent the lock range and capture range as functions of K_d . We can see that the lock range is higher than the capture one and both are incremented when K_d is increased, with the linearity predicted theoretically. However, if K_d is increased, the quality of PLL output signals I and Q worsens due to jitter of the output frequency. To check this fact,

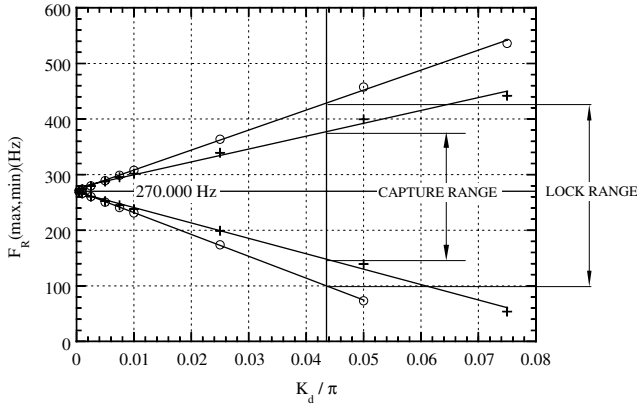


Figure 6. Capture and lock ranges of the DPLL implemented, versus parameter K_d , when an f_{CO} of 270.000 Hz is used.

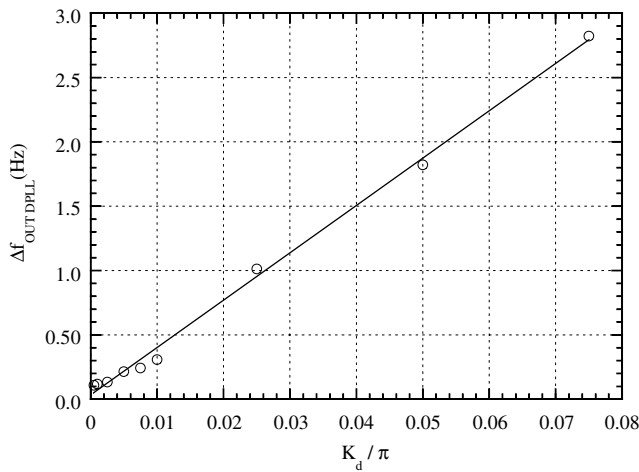


Figure 7. DPLL output jitter as a function of K_d magnitude at a reference frequency of 270.000 Hz.

Table 1. Experimental and theoretical lock range, for different K_d values.

K_d/π	Experimental			Theoretical Δf_L (Hz)
	f_{Lmax} (Hz)	f_{Lmin} (Hz)	Δf_L (Hz)	
0.0005	271.9	268.1	3.8	4
0.0010	273.8	266.1	7.7	8
0.0025	279.6	260.4	19.2	20
0.0050	289.2	250.7	38.5	40
0.0075	298.8	241.0	57.8	60
0.0100	307.8	231.3	76.5	80
0.0250	363.6	173.8	189.8	200
0.0500	457.4	73.0	384.4	400

the frequency stability of signal I is measured using the max-min function of multimeter HP34401A. A reference signal R of 270.000 Hz is used. The spectral bandwidth of signal I in the DSP56002EVM line out is measured for several values of K_d . The results are presented in figure 7. As we expected, the signal obtained is less stable when K_d increases and an effective broadening of the band-pass filter appears when the gain of the PD increases. Then high lock range is in direct opposition to stability of the frequency output of the DPLL. The measured chop frequency drift is less than 2.5 Hz; thus, as shown in table 1, a K_d value of 0.001π is enough to assure lock.

Just as we commented previously, the lock-in, in the

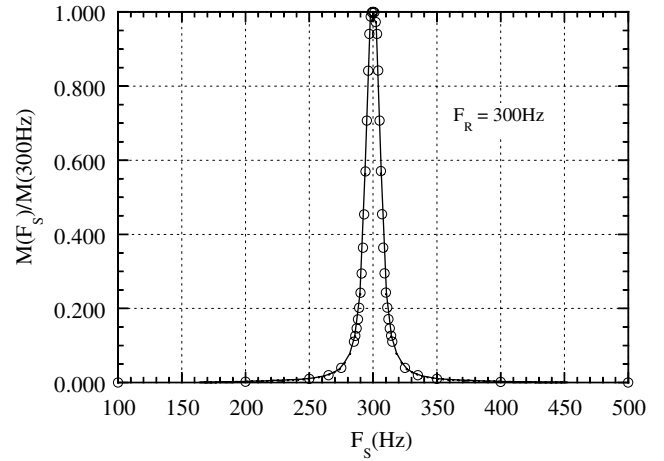


Figure 8. Experimental lock-in frequency response.

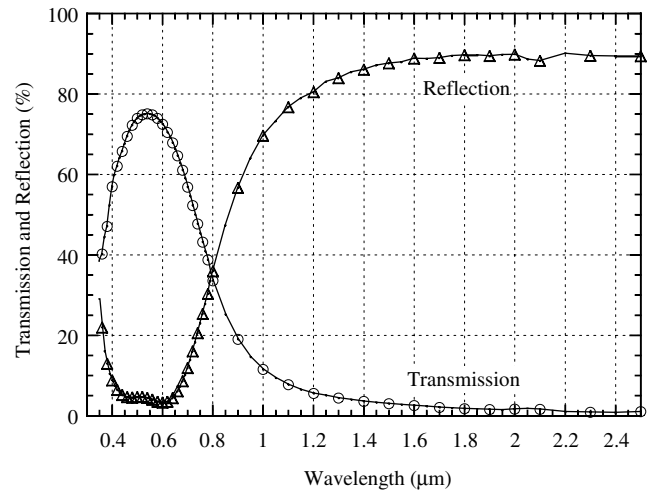


Figure 9. Measured transmission and reflection versus wavelength for a low-emissivity coating glass.

locked state, acts as a band-pass filter, centred on the reference frequency. In figure 8 we show this result. A square wave signal of 300.000 Hz was used as the reference signal R . The HP33120A signal synthesizer was connected to the input signal S to generate a sine wave signal whose frequency was swept in the neighbourhood of 300.000 Hz. In figure 8 are represented the normalized values of output M obtained. The LPF implemented to make these measurements was a second order Butterworth filter with unit gain and cut-off frequency of 5 Hz.

As an example of the operation, figure 9 represents the transmission and reflection values measured by the spectrophotometer for a low-emissivity coating glass.

7. Discussion

As far as the authors are aware, no similar spectrophotometer is available commercially, especially with regard to its robustness, reliability, integrated nature and easiness of the calibration process. Other key features are accuracy, repeatability and high speed of measurement. Excellent results have been obtained working in an industrial environment.

The goal of this work is not to provide new insights or algorithms on the subjects of lock-in amplifiers and PLLs, or

to develop a general-purpose digital lock-in. The goal is to develop a versatile, low-cost, digital lock-in card that could be housed in the spectrophotometer system. Cost is an important parameter, mainly taking into account that two lock-in cards are needed in this system. The use of a DSP allows us to implement the lock-in algorithm by software, which allows flexibility, programmability and easy development. Besides, the user can particularize this lock-in amplifier on the basis of his needs.

The advance in DSP technology is continuous and, nowadays, there are available on the market faster DSPs with more features than the DSP56002. The lock-in algorithm implemented in this DSP can be directly implemented in the latest DSP generations. That will enable the lock-in to be applied to signals sampled at higher frequencies, but this is not necessary in this application because the chop frequency (270 Hz) is low enough.

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