

Improving Sensor Output Characteristics Using Small Adaptive Circuits

G. Zatorre-Navarro, N. Medrano-Marqués, J. Martín-Martínez, S. Celma-Pueyo

Electronic Design Group, Facultad de Ciencias, University of Zaragoza – Spain

Phone: +34 976761240. Fax: +34 976762143

E-mail: {gzatorre, nmedrano}@unizar.es, 465249@cienz.unizar.es, scelma@unizar.es

Abstract

This work studies the application of a mixed-mode electronic neural network to improve the output of nonlinear sensors which show behaviour variations for different samples.

We present an analog current-based neuron model with digital weights, showing its architecture and features. Modifying the algorithm used in off-chip weight fitting main differences of the electronic architecture, compared to the ideal model, are compensated. A small neural network based on the proposed architecture is applied to improve the output of NTC thermistors and GMR sensors, showing good results. Circuit complexity and performance make these systems suitable to be implemented as sensor on-chip compensation modules.

1. Introduction

Artificial Neural Networks (ANNs) are computing tools consisting of small processing elements (artificial neurons), highly interconnected and arranged in layers. The system transfer function is fitted by a training process where input-output data pairs are iteratively presented, adjusting the system free parameters (called weights) that connect inputs from a neuron layer with the preceding neuron layer outputs. ANNs are implemented in several ways, depending on the application requirements. Thus, in systems where size, power consumption and speed are main constraints, electronic analog implementation is a suitable selection [1]. The present-day technology trend to shrinking bias voltages makes difficult to process high-resolution data codified in voltage-mode. In this case, current-mode processing gives better results at lower bias, reducing the power consumption [2].

On the other hand, implementation of reliable long-term and mid-term analog programmable weights results very hard because of mismatching and current offsets. Due to the high accuracy of digital storage in register-based structures, combining both electronic

technologies can improve system performance. Previous works [3] presented the use of mixed-mode multipliers in artificial neuron implementation, showing promising results applied to real problems.

One of the application fields where ANNs are useful is adaptive sensor output improvement, applied to sensors that present nonlinear behaviour in its response, such as negative temperature coefficient resistors mounted on a resistive divider (NTC, Fig. 1) or giant magnetoresistive resistors (GMR, Fig. 2). Another previous works show the use of these processing systems implemented in digital technology [4] or as analog circuits, but applied to classification tasks [5].

This paper shows the application of current-based mixed-mode adaptive circuits to the improvement of non-linear sensors output. In Section 2, the proposed current-based mixed-mode artificial neuron is presented and simulated behaviour is compared to the ideal one. In order to improve neuron operation, some changes in the training process are proposed. Section 3 shows an implementation of an adaptive linearization circuit based on this structure, showing the results for two samples of two different sensors. Finally, some conclusions of this work are presented.

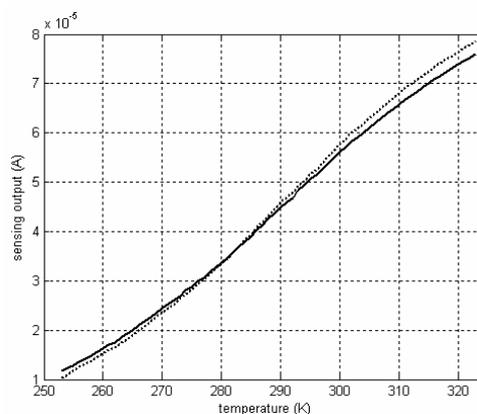


Fig. 1. NTC behavior mounted on a resistive divider (two different samples)

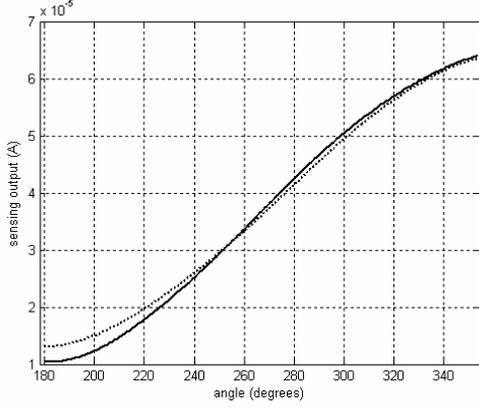


Fig. 2. GMR behavior (two different samples)

2. Current-based Neuron Circuit

The proposed neuron circuit consists of a current-mode four-quadrant analog-digital multiplier plus a current conveyor (CC) that performs the activation function. The main mixed-mode analog-digital neuron building blocks are shown in Fig. 3. Fig. 3a shows the mixed-mode multiplier. Input current is multiplied by a factor lower or equal than 1 using a transistor-based R-2R current ladder [6], [7], controlled by the digital weight bits b_i . Resulting sign is selected modifying the current flow direction: when the weight sign is positive (sign bit is '0'), current enters into the multiplier; however, if weight is negative (sign bit is '1'), the current direction is inverted using the current follower described in [8]. The ideal multiplier output is

$$I_{out2} = I_0 \left(\sum_{n=1}^N \frac{b_n}{2^n} \right) \quad (1)$$

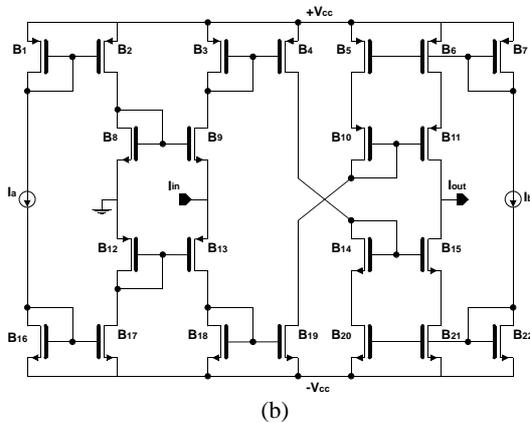
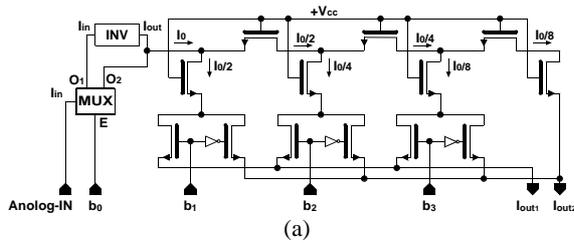


Fig. 3. Main multiplier blocks: (a) analog-digital multiplier; (b) \tanh output circuit

Real multiplier operation is described by

$$out = 0.974865wp - 0.0136726p \quad (2)$$

Where p is the current that inputs to the multiplier, w is the digital weight and out is the current output. Divergences between real and ideal multiplier operation are shown in Fig. 4.

The non-linear operation is executed using a class AB CC (Fig. 3b). Fig. 5 shows circuit operation compared to the ideal \tanh .

The most important neuron non-ideality is due to the non-linear output circuit. As Fig. 5 shows, circuit presents differences in the non-linear corners (upper and lower limits of the central range) plus an additional output offset. Both effects modify the operation of the neural networks implemented using this processing element. In order to fit the network weights and correcting the undesired effects, we have selected a perturbative learning algorithm [9] executed off-line: Network is simulated on a computer in the training phase; next, fitted weights are loaded in the digital storage blocks of the processing elements. The use of a perturbative algorithm is due to the robustness to neuron non-idealities compared to gradient descent-based techniques [10]. Moreover, we have verified that the network improves its performance simulating in the training phase a half of the hidden layer neurons with the inverse of the real non-linear operation function.

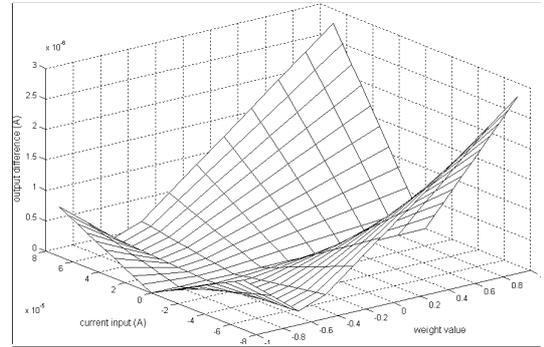


Fig. 4. Differences between the four quadrant mixed-mode multiplier operation and the ideal multiplication

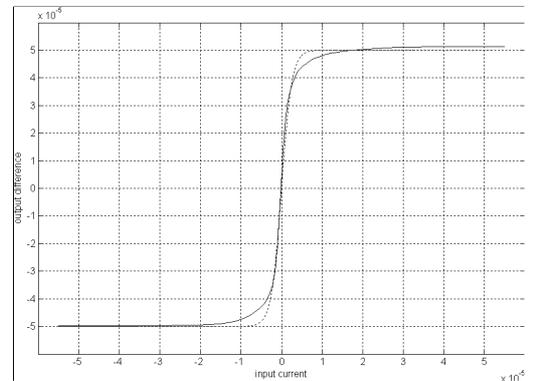


Fig. 5. Class AB current conveyor operation (continuous line) compared to the ideal one (dotted line)

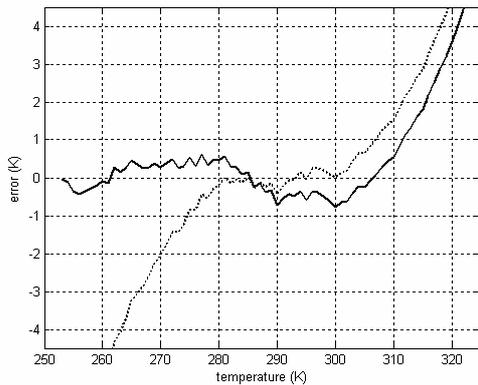
Once the desired performance is reached, the inverted output function is replaced by the real one in the corresponding simulated processor, changing the sign of the corresponding neuron weights. A fast network re-training gives higher performances than using the actual output function in the training phase (Fig. 6). In the example shown in Fig. 6, total error remains lesser than 1K along the sensor span.

3. Sensor output improvement

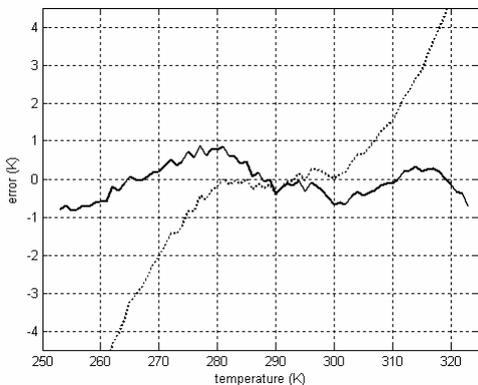
The proposed processing element has been used to extend the linear range of two different sensors: two samples of NTC resistors and two samples of GMR sensors.

3.1. NTC sensors

A neural network with 1 input (nonlinear sensor output), 1 output (correction that must be added to the sensor output) and a two hidden neurons layer is used to extending the linear range of two different NTC sensors (Fig. 1), keeping the error lower than 1K. Each sensor has a data set consisting of 71 temperature-voltage samples in the range of 252-323K degrees. A set of 10 patterns are reserved for testing purposes; the rest is applied in the training cycle. Sensor output errors are compared to the corrected output errors in Fig. 6b and 7



(a)



(b)

Fig. 6. Network output error (continuous line) compared with the sensor output error for an NTC when (a) training is developed normally and (b) a half of the hidden neurons are simulated using the inverse of the actual output

respectively. Fig. 8 shows the resulting corrected output of one of the NTC sensors compared to the sensor output mounted on a resistive divider and the ideal one.

3.2. GMR sensors

As in the previous case, two samples of GMR sensors (Fig. 2) are used to testing the goodness of the proposed technique to extend the linear range of the sensor output. In this case, the number of patterns available along the sensor span (180-355 degrees) is 175; 20 of them are kept for the test/testing stage. Neural network consists of 1 input, 1 output and 4 processing elements in a hidden layer. Figs. 9 and 10 show the errors achieved using this technique compared to the output errors for both sensor samples. Fig. 11 show the resulting corrected output compared to the sensor output and the ideal linear one.

4. Conclusions

This paper shows the application of adaptive mixed-mode circuits to the improvement of non-linear sensors output. The proposed processing element model consists of a current-based artificial neuron with an analog-digital multiplier plus a current conveyor that implements the non-linear output function. Digital

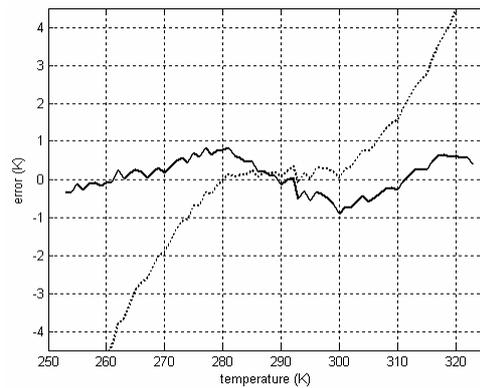


Fig. 7. Output network error (continuous line) compared to the second NTC sensor output. Error remains under the proposed limit

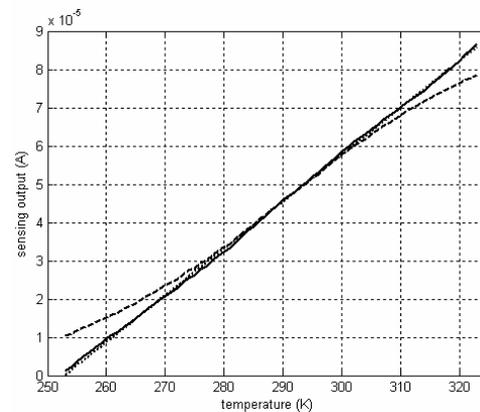


Fig. 8. Output network (continuous line) compared to the sensor output (dashed line) and ideal straight output (dotted line) for an NTC sensor

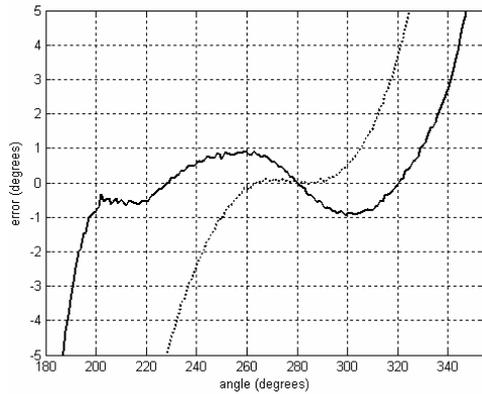


Fig. 9. Output network error (continuous line) compared to the first GMR sensor output (dotted line)

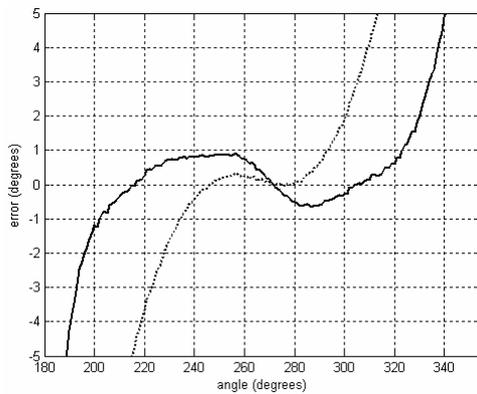


Fig. 10. Output network error (continuous line) compared to the second GMR sensor output (dotted line)

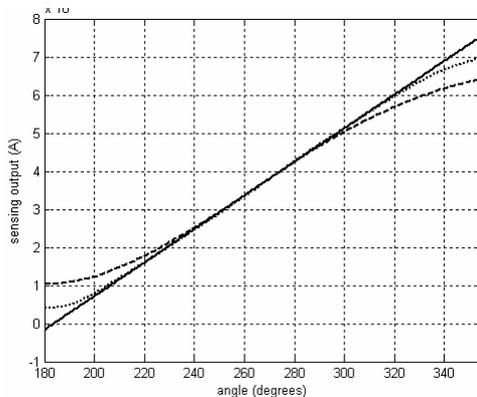


Fig. 11. Output network (dotted line) compared to the sensor output (dashed line) and ideal straight output (continuous line) for a GMR sensor

weight codification allows the long-term storage with the selected accuracy. Our application uses 8-bit precision, multiplying the current inputs using the mixed-mode multiplier. The use of a perturbative training algorithm lets a better weight fitting than gradient descent-based techniques. Moreover, changing the sign of the non-linear output function in a half of the neurons in the simulated training phase improves dramatically the system performance.

Applying this system to the linear output extension of two samples of NTC and GMR, results show very good

results. Table 1 presents the linear output range extension achieved with this technique, assuming a maximum error of 1K for NTC temperature sensors and 1° for angular position GMR sensors.

Sensor	Linear range	Extended range	%
NTC #1	274-308K	252-323K	108
NTC #2	274-308K	252-323K	108
GMR #1	252-305°	198-328°	145
GMR #2	234-292°	202-322°	107

Table 1. Results achieved extending the linear range of each sensor using the proposed neuron model

5. Acknowledgments

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References

- [1] M. Jabri, R. J. Coggins, B. G. Flower, *Adaptive Analog VLSI Neural Systems*, Chapman & Hall, June 1990
- [2] C. Toumazou, F. J. Lidgley, D. G. Haigh, "Analogue IC Design: The Current-Mode Approach", *IEE Circuits and Systems Series 2*. 1990
- [3] C. Lajusticia, N. Medrano, G. Zatorre, B. Martín, "Applying Non-Ideal Mixed Analog-Digital Multipliers in Electronic Processing Circuits Based on Neural Networks", *Proc. 2003 IEEE Conference on Emerging Technologies and Factory Automation, ETFA 2003*, vol. 2, pp. 362-367
- [4] N. Medrano, B. Martín, "A sensor conditioning method for microprocessor based applications", *XVIII Design of Circuits and Integrated Systems Conference, DCIS'02*, pp. 725-730, Santander (Spain), November 2000
- [5] M. Milev, M. Hristov, "Analog Implementation of ANN with Inherent Quadratic Nonlinearity of the Synapses", *IEEE Trans. on Neural Networks*, 2002, vol. 14, n. 5, pp. 1187-1200
- [6] K. Bult, G. Geelen, "An Inherentially Linear and Compact MOST-only Current Division Technique", *IEEE J. Solid-State Circuits* 1992, vol. 27, n. 12, pp. 1730-1735
- [7] M. T. Sanz, B. Calvo, S. Celma, C. Morán, "A Digitally Programmable VGA", *IEEE Midwest Symposium on Circuits and Systems, MWSCAS 2001*, pp. 602-605
- [8] G. Zatorre, P. A. Martínez, C. Aldea, "A New CMOS Class AB Current-Differential Amplifier", *Seminario Annual de Automática, Electrónica Industrial e Instrumentación, SAAEI 2003*, CD-ROM
- [9] M. Jabri, B. Flower, "Weight perturbation: An optimal architecture and learning technique for analog VLSI feedforward and recurrent multilayer networks", *IEEE Transactions on Neural Networks*, vol. 3 no. 1 pp. 154-157, January 1992
- [10] M. Valle, "Analog VLSI implementation of artificial neural networks with Supervised On-Chip Learning", *Analog Integrated Circuits and Signal Processing*, vol. 33 pp. 263-287, 2002