

# Highly-accurate low-voltage source-degenerated-based V-I converter using positive feedback

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A new low-voltage CMOS V-I converter is presented, based on source degeneration. To achieve a highly linear and accurate resistance-based V-I conversion, it makes use of positive feedback  $g_m$ -boosting while body effect compensation is realised through diode-connected transistors. Post-layout results from a 3 V-0.5  $\mu\text{m}$  CMOS design show 0.993% V-to-I conversion accuracy, THD below -60 dB at 10 MHz up to 0.7  $V_{p-p, \text{input}}$  and BW above 400 MHz with 2.1 mW power dissipation.

**Introduction:** One of the simplest and most widely used CMOS V-I converters is the source-degenerated differential pair. Its main limitations to providing an accurate resistance-based linear voltage-to-current conversion are the finite  $g_m$  and the body effect  $g_{mb}$  of the input pair transistors, as shown by its transfer characteristic

$$g_{\text{meff}} = \frac{i}{v_{\text{in}}} = \frac{1}{R + (2/g_m) + (2/g_{mb})} \quad (1)$$

where  $R$  denotes the linear degeneration resistance. Therefore, even if the body effect is neglected, it is required that  $g_m \gg (1/R)$  to obtain a linear V-I relationship inversely proportional to the degeneration resistance. This condition restricts its application as a linear V-I converter to large  $R$  values, and if  $R$  has to be reduced,  $g_m$  has to be accordingly increased, which means higher power consumption.

Focusing on the use of positive feedback to enhance the classical degenerated differential pair performance [1-3], one simple technique to improve linearity without increasing the power consumption is based on the boost of the transconductance  $g_m$ , as shown in the scheme in Fig. 1 (black line), known as the cross-quad [1]. This solution, however, consists of stacked devices, and then requires a noteworthy power supply, not meeting the present day demanded low-voltage requirement. A low-voltage folded version of the cross-quad can be realised as shown in Fig. 1 (grey line). However, in this case, the use of complementary MOS to achieve  $g_m$  neutralisation, as well as the body effect in one of the transistor types in single-well CMOS technology, degrades the linearity performance of the voltage-to-current conversion.

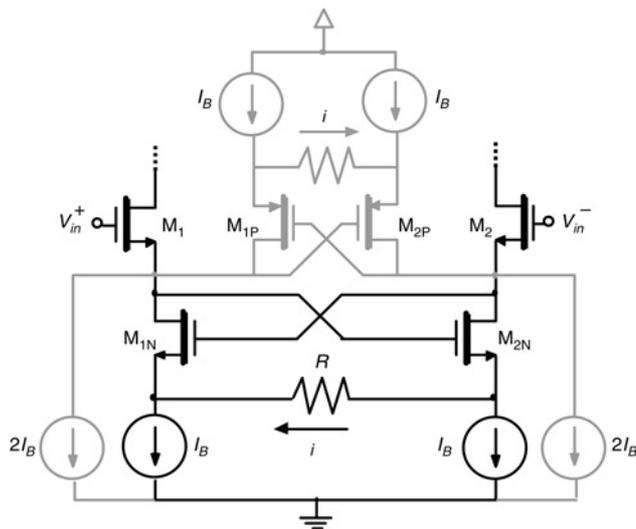


Fig. 1 Cross-quad (black line) and folded cross-quad (grey line)

**V-I converter architecture:** To overcome the aforementioned limitations, the differential stage shown in Fig. 2 is proposed. First, as shown in Fig. 2a, each NMOS input transistor in the classical differential pair is followed by a diode-connected NMOS, so that at nodes A/B body effect compensation is accomplished. Secondly,  $g_m$  neutralisation is done through the use of positive feedback, as shown in Fig. 2b. Each transistor  $M_1, M_2$  in Fig. 2a is split into two identical transistors  $M_1-M_{1N}, M_2-M_{2N}$ , and biasing is adjusted so that all the

pair transistors  $M_1-M_{1N}, M_2-M_{2N}, M_3$  and  $M_4$  drive the same current  $I_B$ . Then, the signal currents of  $M_1, M_{1N}$  are routed to  $M_3$ . This positive feedback path causes the currents and voltage changes in the left side differential pair ( $M_3-M_4$ ) to have the opposite direction to those in Fig. 2a. The effect of this polarity change is that the small-signal transconductances of  $M_3$  and  $M_4$  perform as a negative transconductance with value  $-g_m$ , therefore cancelling the transconductance of  $M_1, M_2$ . As a result, the effective transconductance of this structure is given by  $g_{\text{meff}} = (1/R)$ .

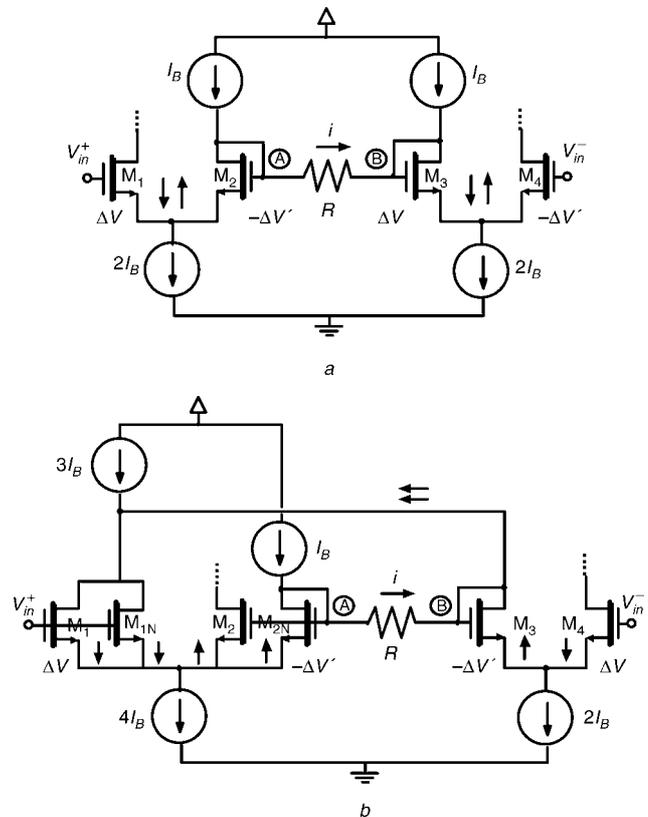


Fig. 2 Proposed V-I converter

a Body effect compensation

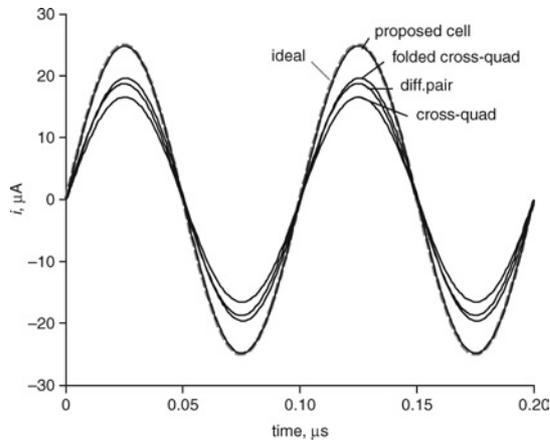
b Complete scheme with body effect and  $g_m$  neutralisation

Besides V-to-I conversion accuracy, from the large-signal point of view the circuit of Fig. 2b is highly linear: assuming that the changes  $\Delta V$  and  $\Delta V'$  in  $M_1-M_2$  cancel those in  $M_3-M_4$ , this leads to an accurate transference of the differential input voltage  $V_{\text{in}}$  to the terminals of resistor  $R$ :  $(V_A - V_B) = (V_{\text{in}}^+ - V_{\text{in}}^-)$ . In consequence, the large-signal voltage-to-current conversion is also given by the linear relationship  $g_{\text{meff}}^{\text{LS}} = (1/R)$ . The output current can be sensed at the drain of  $M_2, M_4$  transistors.

**Implementation and performances:** To evaluate the feasibility of the proposed V-I converter and compare its performances to the other topologies in the literature (classical differential pair, cross-quad and folded cross-quad), all these cells have been designed in a 0.5  $\mu\text{m}$   $p$ -substrate CMOS technology and simulated using Spectre with a level 53 transistor model. Biasing has been implemented through high-swing cascode current mirrors. We have selected for all the circuits a bias current  $I_B = 100 \mu\text{A}$ , a degeneration linear resistance  $R = 20 \text{ k}\Omega$ , pair transistor sizes  $(W/L)_N = (50/1)$ ,  $(W/L)_P = (120/1)$  in ( $\mu\text{m}/\mu\text{m}$ ) and  $V_{DD} = 3 \text{ V}$ , except for the cross-quad, which is operated at 3.5 V. Output current nodes were loaded with  $R_L = 10 \text{ k}\Omega$ .

Fig. 3 shows the transient response of the output current  $i$  for the ideal case  $i = (V_{\text{in}}/R)$  compared to the waveforms for the different considered architectures when applying complementary 10 MHz-0.5  $V_{p-p}$  sinusoidal input signals. The proposed structure achieves a 0.993% accuracy in the V-I conversion, essentially higher than that of all the other topologies based on positive feedback, as can be seen in Fig. 3. Therefore, the proposed cell achieves high V-I conversion accuracy, independently of the value of  $R$ , while simultaneously being

suitable for low-voltage operation and presents a good trade-off between linearity (THD figures at 10 MHz are below  $-60$  dB up to a differential input signal of  $0.7 V_{p-p}$  and below  $-40$  dB up to  $1.6 V_{p-p}$ ), frequency of operation (bandwidth is above 400 MHz), power (2.1 mW) and area consumption. Thus, it can be an appealing choice in applications requiring high precision, such as instrumentation amplifiers where employment of a load resistance  $R_L$  implemented with the same layer as  $R$  results in an accurate and temperature independent gain  $A_v = R_L/R$ . Note that  $R$  (and  $R_L$ ) can be replaced by an array of programmable resistors as in [2], so that tuning of the transconductance is possible for PGA and AGC applications.



**Fig. 3** Output current  $i$  transient response for all cells compared to ideal case

Input signal: 10 MHz,  $1 V_{p-p,diff}$

**Conclusions:** A new V-I converter based on the resistive degenerated differential pair has been designed featuring low-voltage operation, high accuracy and wide bandwidth. Thus, it can be a preferential choice for present-day mixed-signal applications.

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