Low-voltage pseudo-differential transconductor with improved tunability–linearity trade-off

B. Calvo, S. Celma, J. Ramírez-Angulo and M.T. Sanz

A new low-voltage pseudo-differential CMOS transconductor using transistors in the saturation region is presented. It keeps the input common-mode voltage constant, while its transconductance is easily tunable through a DC voltage preserving linearity for a moderate range of G_m values. Post-layout results for a 2.7 V–0.5 μm CMOS design dissipating less than 1.5 mW show a 1:2 G_m tuning range with an almost constant bandwidth over 600 MHz. Total harmonic distortion figures are below −60 dB over the whole range at 10 MHz up to a 100 $\mu A_{p\text{-}p}$ differential output.

Introduction: The ground referred differential pair using transistors in the saturation region with balanced input signals meets the currently demanded low-voltage (LV) requirement. High transconductance G_m values can also be obtained, thus making it an appealing choice for high-frequency operation. However, the only way to tune the G_m – necessary for compensation of fabrication tolerances and to achieve programmability of filter parameters – is through the input common-mode bias voltage V_{CM}. This modifies the transistors' biasing point and directly affects the linearity since the third-harmonic distortion is inversely proportional to the pair transistors' gate overdrive voltage $V_{od} = V_{CM} - V_{TH}$ [1]. In addition, this issue is critical for LV applications where the signal swing, inherently constrained to a small headroom voltage, would be further limited owing to V_{CM} variations.

Transconductance amplifier architecture and performances: To overcome the drawbacks derived from changing V_{CM} for tuning purposes, the pseudo-differential stage shown in Fig. 1 is proposed. Each transistor in the classical pseudo-differential pair is split into matched transistors M_{1A}–M_{1B} and M_{2A}–M_{2B} that form differential pairs. Fully balanced input signals $V_{CM} + (1/2)V_{in}$, $V_{CM} - (1/2)V_{in}$ are applied to M_{1A} and M_{2A}, which act as improved voltage followers thanks to the negative feedback G_m-boosting introduced through M_3 [2]. In consequence, input signals are accurately translated to the source of M_B transistors. Both M_{1B} and M_{2B} gates are driven by a bias voltage $V_{CM} + V_{gain}$. Then, given that M_{1A} and M_{1B} are equally sized and matched, the DC current through M_{1B} will replicate the current in M_{1A}, with a gain which will depend on the voltage V_{gain}. Transistor M_3 takes in M_{1B} current changes.

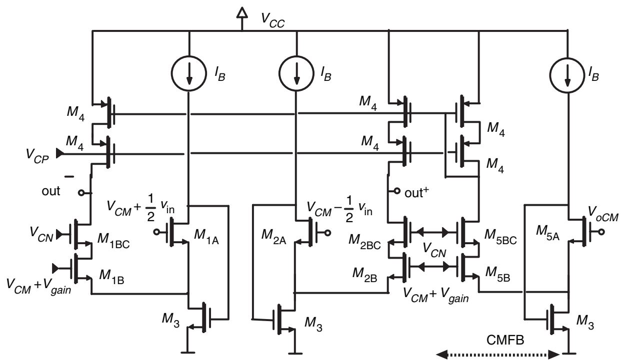

Fig. 1 *Proposed pseudo-differential amplifier*

Straightforward analysis of this stage shows that the output differential current is given by

$$I_O = I^+_{out} - I^-_{out} = 2K(V_{CM} + V_{gain} - V_{TH})V_{in}$$

where V_{TH} is the threshold voltage of M_B transistors and $K = (1/2)\mu C_{OX}(W/L)_B$. This simple scheme thus makes it possible to hold the input common-mode voltage V_{CM} constant, keeping it separate from the transconductance adjustment V_{gain} signal while, as will be shown next, linearity is independent of V_{gain} for a moderate G_m tuning range.

The cell in Fig. 1 has been designed in a standard 0.5 μm CMOS process with a 2.7 V single supply and a bias current of 50 μA. High-swing cascode current mirrors have been used to maximise signal swing while improving mirroring. Cascode transistors, M_{1BC} and M_{2BC}, have been introduced to increase the output resistance up to the M Ω range. To set the adequate output common-mode voltage V_{oCM}, equal to V_{CM}, while properly delivering the required output adaptive current over the whole tuning range, a replica of the single-ended pseudo-differential stage has been employed. The gate of M_{5B} is biased with $V_{CM} + V_{gain}$, while that of M_{5A} is driven by V_{oCM}, whose detection is realised by using two 1 pF capacitors (not shown). The resulting topology is very compact and a maximum ±0.1% V_{CM} variation over the entire G_m tuning range is predicted by simulations. The V_{CM} has been set to 1.7 V so as to obtain a maximum voltage swing of 0.8 $V_{p\text{-}p}$ on each input while maintaining M_A, M_3 in saturation.

Post-layout results using Spectre with a BSIM3v3.2 level 53 transistor model show a 1:2 G_m tuning for V_{gain} varying from −0.1 to +0.1 V, with a bandwidth almost constant above 600 MHz (Fig. 2). For the nominal value $V_{gain} = 0$ V the current through output transistors is $I_{out} = 50$ μA and the power dissipation is 1.08 mW. For $V_{gain} = -0.1$ V and +0.1 V, the currents though output transistors are approximately 25 and 100 μA, and the power consumption 0.88 and 1.46 mW, respectively. To keep moderate consumption, the maximum value for I_{out} that will be considered is 100 μA. The total harmonic distortion figures at 10 MHz (Fig. 3) are below −60 dB over the whole tuning range up to a 100 $\mu A_{p\text{-}p}$ differential output. If we compare these THD levels to those achieved by the conventional pseudo-differential pair with equal transistor sizes, bias current and transconductance values, both structures provide comparable results for $V_{gain} = 0$ V and +0.1 V. However, when reducing V_{od}, i.e. for $V_{gain} = -0.1$ V, the proposed circuit preserves the THD in contrast with the distortion degradation that the classical pseudo-differential pair exhibits, as shown in Fig. 3. The obtained THD improvement for a 100 $\mu A_{p\text{-}p}$ differential output is as high as 10 dB. The CMRR at low frequencies is 77, 73 and 64 dB for $V_{gain} = -0.1$, 0 and +0.1 V, respectively. These CMRR figures are similar to those reported for other CMOS pseudo-differential pairs using transistors in the saturation region [3, 4], all tuned through V_{CM} with the inherent constraints it poses. The input referred noise spectral density is 15 nV/$\sqrt{\text{Hz}}$ at 50 MHz.

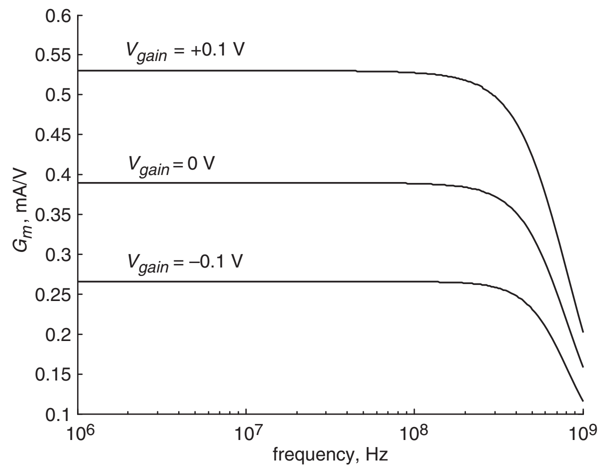

Fig. 2 *Frequency response for $V_{gain} = -0.1$, 0, +0.1 V*

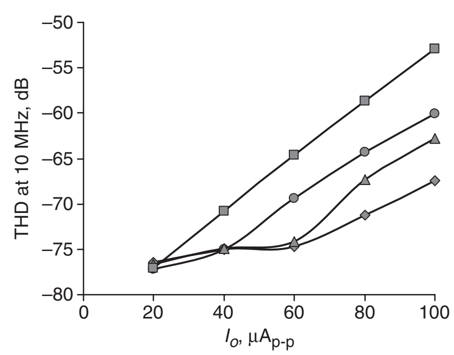

Fig. 3 *THD at 10 MHz*

G_m corresponding to +0.1 V (–◆–), 0 V (–●–) and −0.1 V: (–▲–) proposed and (–■–) classical pseudo-differential pair

Conclusions: A new low-voltage CMOS pseudo-differential pair has been presented, which offers moderate continuous tunability over the video frequency range preserving a good linearity while keeping constant the input common-mode voltage. The proposed cell is thus an appealing choice in present-day mixed signal applications.

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