A New CMOS Class AB Current-Differential Amplifier

G. Zatorre, P.A. Martínez and C. Aldea
Grupo de Diseño Electrónico, Universidad de Zaragoza, 50009 SPAIN
{gzatorre, caldea, pemar2}@unizar.es

***Abstract*—A new CMOS class-AB current amplifier for current-mode analog signal processing is presented.**

Low input impedance, low-power dissipation and differential processing mode are shown by this structure and can be used as a new realization for circuits based on Norton amplifier or current conveyor.

Simulation results show the capability of the presented topology in IF section of wireless applications and the design has been implemented with a standard CMOS process.

***Index Terms*—Current-differential amplifier, analog signal processing.**

I. Introduction

The market of wireless communications demands smaller and lower-cost products and the companies of the sector respond with a progressive introduction of ever more complex chip sets.

The IF section usually comprises pre and post filter programmable gain amplifiers, variable-gain amplifiers (VGA) and band pass filters, which is usually the bottleneck to the dynamic range. These circuits must also provide good linearity for a wide range of signal swing.

Many of the VGA stages and R_m-C filters [1, 2, 3] (using a wideband linear transresistance amplifier) employed in RF transceivers are based on a Norton amplifier [4]. Some of the properties that must be shown by these current amplifiers are: low input impedance, low-voltage and low-power dissipation and, as in telecommunication applications, the signal is processed in a differential form, these amplifiers must been able to handle fully differential signals.

In this paper, a new CMOS class AB current differential amplifier is presented, which can be used as an active component in the filter design [5, 6], basic block in Norton amplifiers, or second-generation current conveyors among other circuits.

The new structure is based on a class AB current mirror due to the fact that class-AB configuration has low-power dissipation (increasing the bias current to signal amplitude ratio) [7], with an improved input resistance by using a positive feedback loop [8] without raising current bias or increasing the transistor size.

The differential input provides a higher versatility to this configuration. In addition, this structure takes advantage of the current-mode operation, the main properties of which are higher frequency and dynamic range.

The proposed amplifier has been implemented in 0.8 μm CMOS technology and operates a 5 V supply, and, the circuit description is presented in section II. In section III, the circuit operation is discussed and the simulation results are shown in section IV.

II. Circuit Descripton

The core of the proposed current amplifier is an improved class AB current follower. In this section, we present the conceptual scheme and the structure used.

A. The Basic Idea

The well-known structure of a class-AB current mirror [9], [10] is shown in Fig.1.

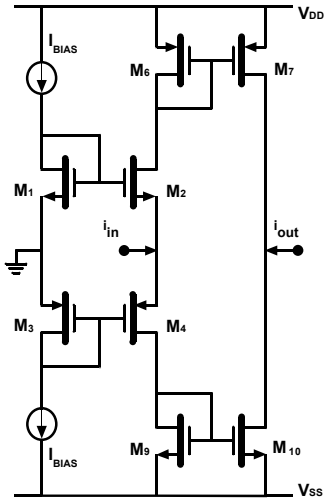

Fig. 1. Class-AB current mirror.

The translinear loop, made up of transistors M1-M4, sets the input voltage equal to ground potential under DC conditions and accurately sets the quiescent current in all the branches allowing control over performance parameters like frequency response, power dissipation, etc.

The main disadvantage of this configuration is the higher input resistance value. However, by using a positive feedback loop the input impedance can be improved [8].

The operation principle is to force the same current in the input and the level shifter stage transistors, allowing variations in the gate voltage. One such structure found using a positive feedback loop is illustrated in Fig. 2.

The main problem of this topology is the absence of a known bias current, the positive feedback loop replaces the bias current sources, and for this reason, it is necessary to implement a bias control system. A bias circuit has been proposed [11] and is shown in the Fig. 2 as a dot square.

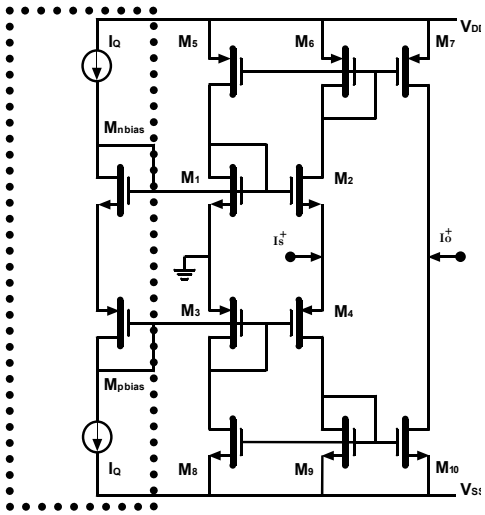

Fig. 2. Topology with a positive feedback loop and proposed bias circuit.

The latter topology will be used to implement a current-differential amplifier by means of a cross-couple structure.

B. The Current Amplifier

The conceptual scheme is shown in Fig. 3, where the detail of block I is described in fig. 2 and corresponds to the non-inverting stage. Block II is detailed in Fig. 4 and corresponds to the inverting stage.

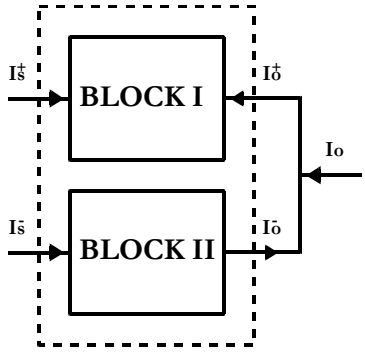

Fig. 3. Proposed structure scheme.

The proposed circuit exhibits a total symmetry between the inverse and the non-inverse inputs, which is not shown in other classical structures [12]. As each input signal path is independent, the system could be characterized by a single input resistance working either in common mode or differential mode, and whose expression is given by: [10]

$$r_{in} = \frac{1}{g_{m4,2}}\left[1 - \frac{g_{m4,2}g_{m10,7}}{g_{m1,3}g_{m9,6}}\right] \qquad (1)$$

Another important characteristic is the topology works in open loop. In this way, compensation schemes are not necessary, and higher frequencies can be reached. Also, this active element is more adaptable than other classic current followers. Nevertheless, the main goal is to offer the possibility of this being a building block in other structures such as Norton amplifiers, CCII+, etc.

In order to improve the current transfer, which is ideal in the absence of second order effects such as mismatching or channel length modulation, a cascode scheme should be used in the output, in particular, the high swing cascode current mirror [13] is a good choice.

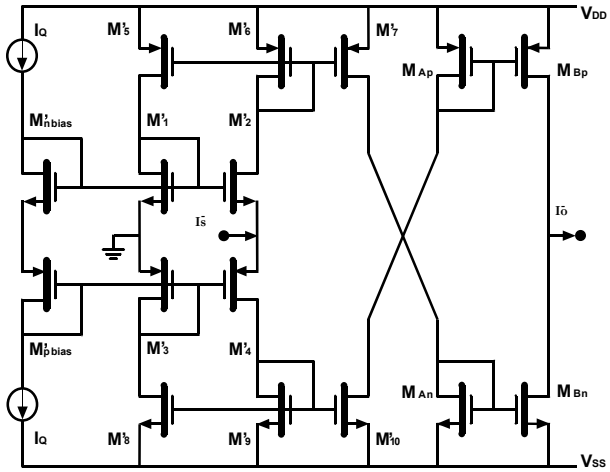

Fig. 4. Inverting stage.

III. CIRCUIT ANALYSIS

If a more detailed frequency analysis is developed, the fact that the inverse signal needs an additional current mirror has its effects on a higher common mode gain, in this way we must add to the random mismatching shown by the current followers the contribution of the mismatching due to the different signal processing paths.

The expression of the current gain to the positive signal is given by:

$$A_I = \frac{g_{m2}g_{m7}}{(g_{m2} + sC_{gs2})(g_{m6} + sC_P)} \qquad (2)$$

where C_P is $C_{gs5} + C_{gs6} + C_{gs7}$.
Likewise, the expression of the current gain to the negative signal is given by

$$A'_I = \frac{g_{m2'}g_{m7'}}{(g_{m2'} + sC'_{gs2})(g_{m6'} + sC'_P)} A_A \qquad (3)$$

and the factor A_A describes the M_A-M_B current mirror gain employed in this signal processing path and which is described by the following expression:

$$A_A = \frac{-\frac{g_{ma}}{g_{mb}}}{1 + s\frac{C_{gsa} + C_{gsb}}{g_{mb}}} \qquad (4)$$

Now, let us consider the mismatching in the previous expressions, denoted as Δ to show the random contribution and ε for the gain error in the additional mirror in the inverse signal path. So, the *dc* current gain of both blocks could be seen as:

$$A_I\big|_{\omega\to 0} = \frac{g_{m7}}{g_{m6}}\left(1 + \frac{1}{2}\Delta\right) = A_o\left(1 + \frac{1}{2}\Delta\right) \quad (5)$$

$$A'_I\big|_{\omega\to 0} = A'_0\left(1 - \frac{1}{2}\Delta\right)(1 \pm \varepsilon) \qquad (6)$$

If an adequate sizing is established between some constituent transistors, the current gain frequency behaviour of each stage could be approximated by a dominant pole. Under this supposition, the differential and the common mode gain of the proposed structure can be expressed as:

$$A_{dm} \cong \frac{A_0}{1 + s/s_a} \qquad (7)$$

$$A_{cm} \cong A_0(\Delta \pm \varepsilon)\frac{(1 + s/s'_b)}{1 + s/s_a} \qquad (8)$$

and the pole and zero are given respectively by:

$$s_a = \frac{g_{m6}g_{m2}}{\sqrt{g_{m2}{}^2 C_p{}^2 + g_{m6}{}^2 C_{gs2}{}^2}} \qquad (9)$$

$$s'_b = (\Delta \pm \varepsilon)\frac{g_{mb}}{(C_{gsa} + C_{gsb})} \qquad (10)$$

Therefore, the CMRR is:

$$CMRR = \left|\frac{A_{dm}}{A_{cm}}\right| \cong \left|\frac{1}{(\Delta \pm \varepsilon)(1 + s/s'_b)}\right| \qquad (11)$$

IV. SIMULATED RESUTS

The proposed circuit has been simulated using a design kit for 0.8 μm double-poly CMOS process. Fig. 5 shows the frequency behaviour results of previous study.

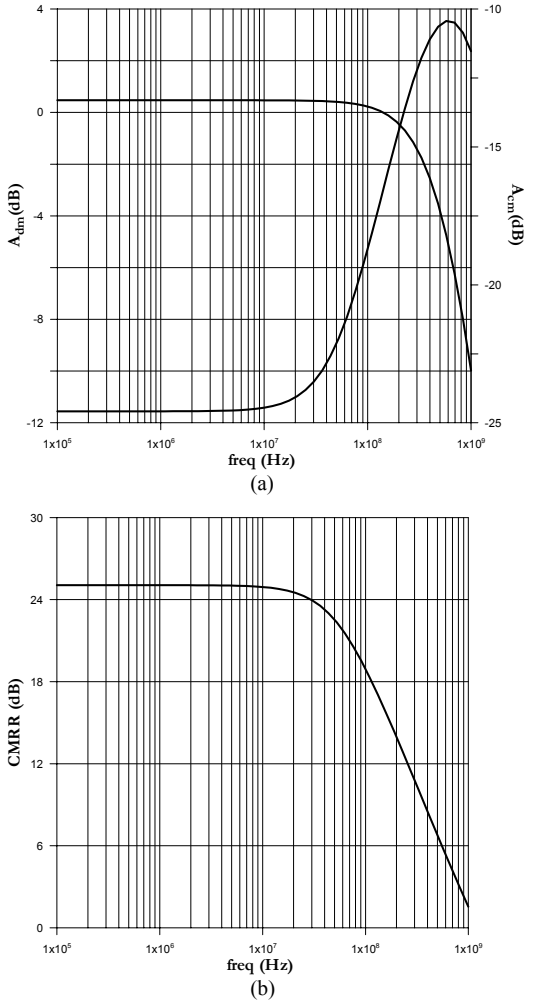

Fig. 5. (a) Frequency response of differential and common mode gain. (b) CMRR

Note that the current-mode operation gives us a higher frequency range.

Some of the main characteristics that are shown by the proposed topology are summarized in Table I.

Parameter	Value
Technology	0.8 μm
V_{DD}-V_{SS}	5 V
GBW	320 MHZ
DC Power	4.8 mW
Rout	28 MΩ
Rin	30 Ω
THD	0.18 %

Table I.

The following graph shows the current transfer of the proposed structure.

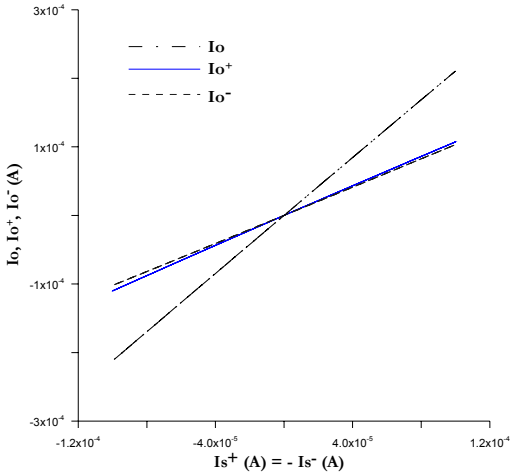

Fig. 6. Current transfer characteristic.

V. Conclusions

This paper describes how to obtain a new current-differential amplifier from a class AB improved current mirror. Experimental results showing a comparative between this structure and commercially available Norton amplifiers will be provided at conference time.

VI. Acknowlements

This work has been partially supported by DGA (P078/2001), CICYT (TIC2002-00636) and MECD (AP2001-2023).

References

[1] H. Elwan, A. M. Soliman and M. Ismail “A CMOS Norton Amplifier-Based Digitally Controlled VGA for Low-Power Wireless Applications”. IEEE Trans. Circuits and Systems-II, vol. 48, n. 3, pp.245-254, 2001

[2] P-H Lu, C-Y. Wu and M-K Tsai, “Design Techniques Tunable Transresistance-C VHF Bandpass Filters”. IEEE J. Solid-State Circuits, vol. 29, n. 9, pp. 1058-1067, 1994.

[3] P-H Lu, C-Y. Wu and M-K Tsai, “Design Techniques for VHF/UHF High-Q Tunable Bandpass Filters Using Simple CMOS Inverter-Based Transresistance Amplifier”. IEEE J. Solid-State Circuits, vol. 31, n. 5, pp. 719-725, 1996.

[4] T. M. Frederiksen, W. F. Davis and D. W. Zobel “A New Current-Differencing Single-Supply Operational Amplifier”. IEEE J. Solid-State Circuits, vol. SC-6, pp. 340-347, 1971

[5] S. Celma, J. Sabadell, P.A. Martínez. “Universal Filter Using Unit-Gain Cells”. Electronics Letters, vol. 31, n. 22, pp 1817-1818, 1995.

[6] H. Alzaher, M. Ismail. “Current Mode Universal Filter Using Unity Gain Cells”. Electronics Letters, vol. 35, n. 25, pp 2198-2200, 1999.

[7] S. Kawahito and Y. Tadokoro, “CMOS Class-AB Current Mirror for Precision Current-Mode Analog-Signal-Processing Elements”. IEEE Trans. Circuits and Systems-II, vol. 43, n. 12, pp. 843-845, 1996.

[8] Z. Wang, “Wideband Class AB (push-pull) Current Amplifier in CMOS Technology”. Electronics Letters, vol. 26, n. 8, pp. 543-545, 1990.

[9] E. Brunn, “Analytical Expressions for Harmonic Distortion at Low Frequencies due to Device Mismatch in CMOS Current Mirrors”. IEEE Trans. Circuits and Systems-II, vol. 46, n. 7, pp. 937-941, 1999.

[10] G. Palmisano, G. Palumbo and S. Pennisi. “CMOS current amplifiers”. Kluwer Academic Publishers, 1999.

[11] C. Aldea and P. A. Martínez, “CMOS Class-AB Current Mirrors and Followers: Systems in Harmony”. SAAEI Vol. I pp. 123-125, 2002.

[12] K. N. Salama, A. M. Soliman. “CMOS Operational Transresistance Amplifier for Analog Signal Processing”. Microelectronics Journal 30, pp. 235-245, 1999.

[13] P. J. Crawley, G. W. Roberts. “High-Swing MOS Current Mirror with Arbitrarily High Output Resistance”. Electronics Letters, Vol.28, No. 4, pp.361-363, 1992.